General Purpose Base Board for Gate Driver Core 2SC0108T

<table>
<thead>
<tr>
<th>Application</th>
<th>General purpose drives, UPS, solar power and others</th>
</tr>
</thead>
<tbody>
<tr>
<td>Specification</td>
<td>Suitable for IGBT power modules in various housings</td>
</tr>
<tr>
<td></td>
<td>Up to 1200V DC-link voltage</td>
</tr>
<tr>
<td></td>
<td>Electrical interfaces</td>
</tr>
<tr>
<td></td>
<td>Basic Active Clamping</td>
</tr>
<tr>
<td></td>
<td>Short-circuit detection with Soft Shut Down (SSD)</td>
</tr>
<tr>
<td>Author</td>
<td>High-Power Application Engineering Department</td>
</tr>
<tr>
<td>Document Number</td>
<td>RDHP-1415</td>
</tr>
<tr>
<td>Revision¹</td>
<td>A.3</td>
</tr>
</tbody>
</table>

¹ The letter refers to the hardware revision. The number refers to the documentation revision.
Scope

This application proposal provides a circuit design for a general purpose base board for driving various IGBT power modules.

The main features of the design are:

- Suitable for IGBT power modules in various housings such as 17mm dual, 17mm six-pack, 62mm, PrimePACK™, etc. with a maximum blocking voltage of 1700V
- (Optional) Basic Active Clamping
- Short-circuit detection with Soft Shut Down (SSD)
- Electrical command inputs and status outputs
- 0V/15V command input logic
- 0V/15V status output logic
- Minimum pulse suppression (optional)
- Adjustable blocking time
- 15V supply voltage
- Single PCB solution with soldered-in gate driver core

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Application Conditions

The design is proposed for the following application conditions:

- General purpose applications and IGBT power modules
- Adaptations such as adjustment of gate resistors can easily be done
## Design Description

In addition to the following design description, reference to the datasheet(s) and application manual of the 2SC0108T gate driver family is recommended.

### Gate Resistors

Gate resistor values are not explicitly given as they depend on the IGBT power module used and on the application. Gate resistors of either SMD (size 1206) or THT (size PR02) package can be selected.

#### Turn-on gate resistors:

<table>
<thead>
<tr>
<th>Channel</th>
<th>SMD Package</th>
<th>THT Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>R118a ... R118d</td>
<td>R116</td>
</tr>
<tr>
<td>2</td>
<td>R218a ... R218d</td>
<td>R216</td>
</tr>
</tbody>
</table>

#### Turn-off gate resistors:

<table>
<thead>
<tr>
<th>Channel</th>
<th>SMD Package</th>
<th>THT Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>R117a ... R117d</td>
<td>R115</td>
</tr>
<tr>
<td>2</td>
<td>R217a ... R217d</td>
<td>R215</td>
</tr>
</tbody>
</table>

The gate resistors must be determined and assembled by the user. Minimum required gate resistor values are defined in the datasheet of the gate driver 2SC0108T.

### V\textsubscript{CEsat} Monitoring

In the schematic and bill of material, the resistor networks of the V\textsubscript{CEsat} monitoring function are marked with "N.A." (not assembled), as their concrete value depends on the IGBT power module and applied DC-link voltage.

Recommended values are listed in the following table:

<table>
<thead>
<tr>
<th>IGBT voltage</th>
<th>Max. DC-link voltage</th>
<th>R101</th>
<th>R102 to R113</th>
<th>R201</th>
<th>R202 to R213</th>
</tr>
</thead>
<tbody>
<tr>
<td>600V</td>
<td>400V</td>
<td>62kΩ</td>
<td>47kΩ</td>
<td>62kΩ</td>
<td>47kΩ</td>
</tr>
<tr>
<td>1200V</td>
<td>800V</td>
<td>120kΩ</td>
<td>100kΩ</td>
<td>120kΩ</td>
<td>100kΩ</td>
</tr>
<tr>
<td>1700V</td>
<td>1200V</td>
<td>120kΩ</td>
<td>150kΩ</td>
<td>120kΩ</td>
<td>150kΩ</td>
</tr>
</tbody>
</table>

Recommended values of the blanking capacitors C100 and C200 as well as further details of the V\textsubscript{CEsat} monitoring function are described in the corresponding application manual of the gate driver 2SC0108T.

### Soft Shut Down (SSD)

The gate driver cores 2SC0108T with SCALE-2+ chip set feature an SSD function, which reduces the turn-off $\frac{\Delta i}{\Delta t}$ to limit V\textsubscript{CE} overvoltage spikes as soon as a short-circuit condition is detected. An excessive turn-off overvoltage is therefore avoided and the IGBT is turned off within its safe operating area.

The SSD function is only active under short-circuit conditions, but not under normal operating conditions (e.g. at nominal current or in over-current conditions), i.e. it is triggered by the V\textsubscript{CEsat} monitoring function.

The SSD function may also have performance limitations, such as at high DC-link voltages and/or high commutation loop stray inductances. If the application is operated at these boundary conditions, it is recommended to implement Basic Active Clamping.
For further details concerning the SSD function refer to the application manual of the gate driver core 2SC0108T.

**Basic Active Clamping**

Active clamping is a technique designed to partially turn on the IGBT in case the collector-emitter voltage exceeds a predefined threshold. The IGBT is then kept in linear operation. Basic Active Clamping topologies implement a single feedback path from the IGBT's collector through transient voltage suppressor (TVS) diodes to the IGBT gate.

In the schematic and bill of material the TVS networks (D103 to D108 and D203 to D208) are marked with “N.A.” (not assembled) as their specific value depends on the IGBT power module and applied DC-link voltage. Recommended values are listed in the following table.

<table>
<thead>
<tr>
<th>IGBT voltage</th>
<th>Max. DC-link voltage</th>
<th>D102, D202</th>
<th>D103 ... D107, D203 ... D207</th>
<th>D108, D208</th>
</tr>
</thead>
<tbody>
<tr>
<td>600V</td>
<td>400V</td>
<td>STPS340U</td>
<td>P6SMJ70A</td>
<td>P6SMBJ70CA</td>
</tr>
<tr>
<td>1200V</td>
<td>800V</td>
<td>STPS340U</td>
<td>SMBJ130A-E3</td>
<td>SMBJ130CA-E3</td>
</tr>
<tr>
<td>1700V</td>
<td>1200V</td>
<td>STPS340U</td>
<td>P6SMBJ220A</td>
<td>P6SMBJ220CA</td>
</tr>
</tbody>
</table>

Basic Active Clamping is recommended as an additional option in case the Soft Shut Down (SSD) function of the gate driver core is used. For further details and alternative TVS diodes refer to the application manual of the gate driver core 2SC0108T.

**Minimum Pulse Suppression**

This design possesses the option to implement a minimum pulse suppression with a time constant $\tau$. If required the minimum pulse suppression can be set by adjusting $C300$ and $C301$. The time constant $\tau$ is given by the following equations:

$$
\tau_1 = 0.88k\Omega \cdot C300 \\
\tau_2 = 0.88k\Omega \cdot C301
$$

Recommended values of $C300$ and $C301$ are in the range of 100pF ($\tau_x = 88$ns) to 470pF ($\tau_x = 414$ns), depending on actual application conditions.

**Blocking Time**

During the blocking time the gate driver ignores incoming command signals. The blocking time starts once a fault was detected by the gate driver’s secondary side (undervoltage lock-out or a short-circuit event) or when an undervoltage condition ends on the primary side.

The terminal TB allows the default blocking time of typically 99ms (R318) to be reduced by connecting an optional external resistor to GND. The external resistor $R_b$ needs to be equal or larger than 129k$\Omega$ to fulfill the following formula:

$$(R_b + 6.8k\Omega) || 150k\Omega \approx T_b + 51ms \text{ with } 20ms < T_b < 99ms$$

In case the terminal TB is directly shorted to GND ($R_b = 0\Omega$), the blocking time is set to its minimum value as described in the datasheet of the gate driver core 2SC0108T.
## Interfaces

### Electrical Interfaces

<table>
<thead>
<tr>
<th>X3 Pin</th>
<th>Designation</th>
<th>Description</th>
<th>X3 Pin</th>
<th>Designation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>n.c.</td>
<td>Not connected</td>
<td>2</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>3</td>
<td>n.c.</td>
<td>Not connected</td>
<td>4</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>5</td>
<td>VCC</td>
<td>15V supply (referenced to GND)</td>
<td>6</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>7</td>
<td>VCC</td>
<td>15V supply (referenced to GND)</td>
<td>8</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>9</td>
<td>SO2</td>
<td>Status output channel 2</td>
<td>10</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>11</td>
<td>INB</td>
<td>Command input channel 2</td>
<td>12</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>13</td>
<td>SO1</td>
<td>Status output channel 1</td>
<td>14</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>15</td>
<td>INA</td>
<td>Command input channel 1</td>
<td>16</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>17</td>
<td>MOD</td>
<td>Mode selector</td>
<td>18</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>19</td>
<td>TB</td>
<td>Set blocking time</td>
<td>20</td>
<td>GND</td>
<td>Ground</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>X1 Pin</th>
<th>Designation</th>
<th>Description</th>
<th>X2 Pin</th>
<th>Designation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>C1</td>
<td>Collector channel 1</td>
<td>1</td>
<td>C2</td>
<td>Collector channel 2</td>
</tr>
<tr>
<td>2</td>
<td>n.c.</td>
<td>Not connected</td>
<td>2</td>
<td>n.c.</td>
<td>Not connected</td>
</tr>
<tr>
<td>3</td>
<td>n.c.</td>
<td>Not connected</td>
<td>3</td>
<td>n.c.</td>
<td>Not connected</td>
</tr>
<tr>
<td>4</td>
<td>n.c.</td>
<td>Not connected</td>
<td>4</td>
<td>n.c.</td>
<td>Not connected</td>
</tr>
<tr>
<td>5</td>
<td>n.c.</td>
<td>Not connected</td>
<td>5</td>
<td>n.c.</td>
<td>Not connected</td>
</tr>
<tr>
<td>6</td>
<td>G1</td>
<td>Gate channel 1</td>
<td>6</td>
<td>G2</td>
<td>Gate channel 2</td>
</tr>
<tr>
<td>7</td>
<td>VE1</td>
<td>Emitter channel 1</td>
<td>7</td>
<td>VE2</td>
<td>Emitter channel 2</td>
</tr>
</tbody>
</table>
CAD Data

The set of CAD data, which includes the circuit schematics, Gerber files, BOM and Pick-and-Place file are available as separate documents bundled together with this documentation.

Layout Example

An example for a suitable layout is shown in the following picture. The recommended PCB thickness is 1.55mm (for gate driver cores with terminal length of 2.54mm) and 2.0mm (for gate driver cores with terminals length ≥3.1mm).
Switching Characteristic

**Turn-On/ Off**

The following measurement examples were carried out at room temperature with the IGBT power module FF300R17KE3 from Infineon Technologies ($R_{\text{on}} = 4.7\,\Omega$ and $R_{\text{off}} = 4.7\,\Omega$) in a double-pulse test using a half-bridge topology setup with an initial DC-link voltage of $1200\,\text{VDC}$. The adjusted load current is either $300\,\text{A (I}_{\text{nom}}$) or $600\,\text{A (2x I}_{\text{nom}}$).

Channel assignment:
- Channel C2: Collector current ($1\,\text{V} \equiv 1\,\text{A}$)
- Channel C3: Collector-emitter voltage
- Channel C4: Gate-emitter voltage

Turn-off bottom side ($I_{\text{nom}}$)

Turn-on bottom side ($I_{\text{nom}}$)

Turn-off bottom side (2x $I_{\text{nom}}$)

Turn-on bottom side (2x $I_{\text{nom}}$)
Short-Circuit

The following measurement example was carried out at room temperature with the IGBT power module FF300R17KE3 from Infineon Technologies (R_{Gon} = 4.7\,\Omega \text{ and } R_{Goff} = 4.7\,\Omega) with an initial DC-link voltage of 1200\,V_{DC}.

Channel assignment:

Channel C1: Command input signal
Channel C2: Collector current (1\,V \triangleq 1A)
Channel C3: Collector-emitter voltage
Channel C4: Gate-emitter voltage

Bottom side
Handling

To avoid possible failures caused by ESD, a handling- and assembly-process with persistent ESD protection is necessary /3/.

References

/1/ 2SC0108T2xx-17 Data Sheet, Power Integrations
/2/ 2SC0108T2xx-17 Description & Application Manual, Power Integrations
/3/ Application Note AN-0902, “Avoiding ESD with CONCEPT Drivers”, Power Integrations

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