## General Purpose Base Board for Gate Driver Core 2SC0106T

<table>
<thead>
<tr>
<th>Application</th>
<th>General purpose drives, UPS, solar power and others</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Specification</strong></td>
<td>Suitable for IGBT power modules in various housings</td>
</tr>
<tr>
<td></td>
<td>Up to 800V DC-link voltage</td>
</tr>
<tr>
<td></td>
<td>Electrical interfaces</td>
</tr>
<tr>
<td></td>
<td>Basic Active Clamping</td>
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<td></td>
<td>Short-circuit detection with Soft Shut Down (SSD)</td>
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<tr>
<td><strong>Author</strong></td>
<td>High-Power Application Engineering Department</td>
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<tr>
<td><strong>Document Number</strong></td>
<td>RDHP-1423</td>
</tr>
<tr>
<td><strong>Revision</strong>¹</td>
<td>A.4</td>
</tr>
</tbody>
</table>

¹ The letter refers to the hardware revision. The number refers to the documentation revision.
Scope

This application proposal provides a circuit design for a general purpose base board for driving various IGBT power modules.

The main features of the design are:

- Suitable for IGBT power modules in various housings such as 17mm dual, 17mm six-pack, 62mm, PrimePACK™, etc. with a maximum blocking voltage of 1200V
- (Optional) Basic Active Clamping
- Short-circuit detection with Soft Shut Down (SSD)
- Electrical command inputs and status outputs
- 0V/15V command input logic
- 0V/15V status output logic
- Minimum pulse suppression (optional)
- Adjustable blocking time
- 15V supply voltage
- Single PCB solution with soldered-in gate driver core

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Application Conditions

The design is proposed for the following application conditions:

- General purpose applications and IGBT power modules
- Adaptations such as adjustment of gate resistors can easily be done
Design Description

In addition to the following design description, reference to the datasheet(s) and application manual of the 2SC0106T gate driver family is recommended.

Gate Resistors

Gate resistor values are not explicitly given as they depend on the IGBT power module used and on the application. Gate resistors of either SMD (size 1206) or THT (size PR02) package can be selected. The turn-on and turn-off gate resistors are setup according to the following scheme (x = 1 for gate resistors for channel 1 and x = 2 for channel 2):

**SMD gate resistors**

\[ R_{Gon} = \frac{R_a \times R_b}{R_a + R_b} \quad \text{and} \quad R_{Goff} = R_a \]

with \( R_a^{-1} = Rx30a^{-1} + Rx30b^{-1} + Rx30c^{-1} + Rx30d^{-1} \) and \( R_b^{-1} = Rx40a^{-1} + Rx40b^{-1} + Rx40c^{-1} + Rx40d^{-1} \)

**THT gate resistors**

\[ R_{Gon} = Rx20 \times Rx21 / (Rx20 + Rx21) \quad \text{and} \quad R_{Goff} = Rx21 \]

The gate resistors must be determined and assembled by the user. Minimum required gate resistor values are defined in the datasheet of the gate driver 2SC0106T.

V\textsubscript{CEsat} Monitoring

In the schematic and bill of material, the resistor networks of the V\textsubscript{CEsat} monitoring function are marked with “N.A.” (not assembled), as their concrete value depends on the IGBT power module and applied DC-link voltage.

Recommended values are listed in the following table:

<table>
<thead>
<tr>
<th>IGBT voltage</th>
<th>Max. DC-link voltage</th>
<th>R100</th>
<th>R101 to R108</th>
<th>R200</th>
<th>R201 to R208</th>
</tr>
</thead>
<tbody>
<tr>
<td>600V</td>
<td>400V</td>
<td>62kΩ</td>
<td>82kΩ</td>
<td>62kΩ</td>
<td>82kΩ</td>
</tr>
<tr>
<td>1200V</td>
<td>800V</td>
<td>120kΩ</td>
<td>150kΩ</td>
<td>120kΩ</td>
<td>150kΩ</td>
</tr>
</tbody>
</table>

Recommended values of the blanking capacitors C103 and C203 as well as further details of the V\textsubscript{CEsat} monitoring function are described in the corresponding application manual of the gate driver 2SC0106T.

Soft Shut Down (SSD)

The gate driver cores 2SC0106T with SCALE-2+ chip set feature an SSD function, which reduces the turn-off \( \frac{dV}{dt} \) to limit V\textsubscript{CEsat} overvoltage spikes as soon as a short-circuit condition is detected. An excessive turn-off overvoltage is therefore avoided and the IGBT is turned off within its safe operating area.

The SSD function is only active under short-circuit conditions, but not under normal operating conditions (e.g. at nominal current or in over-current conditions), i.e. it is triggered by the V\textsubscript{CEsat} monitoring function.

The SSD function may also have performance limitations, such as at high DC-link voltages and/or high commutation loop stray inductances. If the application is operated at these boundary conditions, it is recommended to implement Basic Active Clamping.
Basic Active Clamping

Active clamping is a technique designed to partially turn on the IGBT in case the collector-emitter voltage exceeds a predefined threshold. The IGBT is then kept in linear operation. Basic Active Clamping topologies implement a single feedback path from the IGBT's collector through transient voltage suppressor (TVS) diodes to the IGBT gate.

In the schematic and bill of material the TVS networks (D101 to D106 and D201 to D206) are marked with “N.A.” (not assembled) as their specific value depends on the IGBT power module and applied DC-link voltage. Recommended values are listed in the following table.

<table>
<thead>
<tr>
<th>IGBT voltage</th>
<th>Max. DC-link voltage</th>
<th>D109, D209</th>
<th>D101 ... D106, D201 ... D206</th>
</tr>
</thead>
<tbody>
<tr>
<td>600V</td>
<td>400V</td>
<td>STPS340U</td>
<td>P6SMBJ70A</td>
</tr>
<tr>
<td>1200V</td>
<td>800V</td>
<td>STPS340U</td>
<td>SMBJ130A-E3</td>
</tr>
</tbody>
</table>

Basic Active Clamping is recommended as an additional option in case the Soft Shut Down (SSD) function of the gate driver core is used.

Minimum Pulse Suppression

This design possesses the option to implement a minimum pulse suppression with a time constant $\tau$. If required the minimum pulse suppression can be set by adjusting C304 and C305. The time constant $\tau$ is given by the following equations:

$$\tau_1 = 0.88k\Omega \cdot C304$$

$$\tau_2 = 0.88k\Omega \cdot C305$$

Recommended values of C304 and C305 are in the range of 100pF ($\tau_x = 88$ns) to 470pF ($\tau_x = 414$ns), depending on actual application conditions.

Blocking Time

During the blocking time the gate driver ignores incoming command signals. The blocking time starts once a fault was detected by the gate driver's secondary side (undervoltage lock-out or a short-circuit event) or when an undervoltage condition ends on the primary side.

The terminal TB allows the default blocking time of typically 99ms (R307) to be reduced by connecting an optional external resistor to GND. The external resistor $R_b$ needs to be equal or larger than 129k$\Omega$ to fulfill the following formula:

$$(R_b + 6.8k\Omega) || 150k\Omega \leq T_b + 51ms \text{ with } 20ms < T_b < 99ms$$

In case the terminal TB is directly shorted to GND ($R_b = 0\Omega$), the blocking time is set to its minimum value as described in the datasheet of the gate driver core 2SC0106T.
## Interfaces

### Electrical Interfaces

<table>
<thead>
<tr>
<th>Pin</th>
<th>Designation</th>
<th>Description</th>
<th>Pin</th>
<th>Designation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>n.c.</td>
<td>Not connected</td>
<td>2</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>3</td>
<td>n.c.</td>
<td>Not connected</td>
<td>4</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>5</td>
<td>VCC</td>
<td>15V supply (referenced to GND)</td>
<td>6</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>7</td>
<td>VCC</td>
<td>15V supply (referenced to GND)</td>
<td>8</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>9</td>
<td>n.c.</td>
<td>Not connected</td>
<td>10</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>11</td>
<td>INB</td>
<td>Command input channel 2</td>
<td>12</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>13</td>
<td>SO</td>
<td>Combined status output</td>
<td>14</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>15</td>
<td>INA</td>
<td>Command input channel 1</td>
<td>16</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>17</td>
<td>n.c.</td>
<td>Not connected</td>
<td>18</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>19</td>
<td>TB</td>
<td>Set blocking time</td>
<td>20</td>
<td>GND</td>
<td>Ground</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Pin</th>
<th>Designation</th>
<th>Description</th>
<th>Pin</th>
<th>Designation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>C1</td>
<td>Collector channel 1</td>
<td>1</td>
<td>C2</td>
<td>Collector channel 2</td>
</tr>
<tr>
<td>2</td>
<td>n.c.</td>
<td>Not connected</td>
<td>2</td>
<td>n.c.</td>
<td>Not connected</td>
</tr>
<tr>
<td>3</td>
<td>n.c.</td>
<td>Not connected</td>
<td>3</td>
<td>n.c.</td>
<td>Not connected</td>
</tr>
<tr>
<td>4</td>
<td>n.c.</td>
<td>Not connected</td>
<td>4</td>
<td>n.c.</td>
<td>Not connected</td>
</tr>
<tr>
<td>5</td>
<td>G1</td>
<td>Gate channel 1</td>
<td>5</td>
<td>G2</td>
<td>Gate channel 2</td>
</tr>
<tr>
<td>6</td>
<td>VE1</td>
<td>Emitter channel 1</td>
<td>6</td>
<td>VE2</td>
<td>Emitter channel 2</td>
</tr>
</tbody>
</table>
**CAD Data**

The set of CAD data, which includes the circuit schematics, Gerber files, BOM and Pick-and-Place file are available as separate documents bundled together with this documentation.

**Layout Example**

An example for a suitable layout is shown in the following picture. The recommended PCB thickness is 1.55mm.
Switching Characteristic

Switching Examples

The measurement examples shown with the IGBT power module FF450R12KT4 from Infineon Technologies ($R_{Gon} = 4.3\,\Omega$ and $R_{Goff} = 4.3\,\Omega$) were carried out in a double pulse test using a half-bridge topology setup at room temperature with an initial DC-link voltage of 800VDC. The adjusted load current is 900A ($2\times I_{nom}$). Basic Active Clamping (BAC) was implemented for these tests.

Channel assignment:
Channel C1: Status output (short-circuit only)  
Channel C2: Collector current ($1\,V \cong 1A$)  
Channel C3: Collector-emitter voltage  
Channel C4: Gate-emitter voltage

Turn-on top side ($2\times I_{nom}$)  
Turn-off top side ($2\times I_{nom}$)  
Short-circuit top side
Handling

To avoid possible failures caused by ESD, a handling- and assembly-process with persistent ESD protection is necessary /3/.

References

/1/ 2SC0106T2Ax-12 Data Sheet, Power Integrations
/2/ 2SC0106T2Ax-12 Description & Application Manual, Power Integrations
/3/ Application Note AN-0902, “Avoiding ESD with CONCEPT Drivers”, Power Integrations

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