General Purpose Base Board for Gate Driver Core 2SC0535T

<table>
<thead>
<tr>
<th>Application</th>
<th>General purpose drives, traction, wind power and others</th>
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<tbody>
<tr>
<td>Specification</td>
<td>Suitable for 3.3kV IGBT power modules in various housings</td>
</tr>
<tr>
<td></td>
<td>Up to 2200V DC-link voltage</td>
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<tr>
<td></td>
<td>Electrical interfaces</td>
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<tr>
<td></td>
<td>Dynamic Advanced Active Clamping</td>
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<tr>
<td></td>
<td>Short-circuit detection</td>
</tr>
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<table>
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<tr>
<th>Author</th>
<th>High-Power Application Engineering Department</th>
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<tr>
<td>Document Number</td>
<td>RDHP-1517</td>
</tr>
<tr>
<td>Revision¹</td>
<td>A.2</td>
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</table>

¹ The letter refers to the hardware revision. The number refers to the documentation revision.
Scope

This application proposal provides a circuit design for a general purpose base board for driving various IGBT power modules.

The main features of the design are:

- Suitable for IGBT power modules in various housings such as 130mm x 140mm, 190mm x 140mm, etc. with a blocking voltage of 3300V
- Dynamic Advanced Active Clamping
- Short-circuit detection
- Electrical command inputs and status outputs
- 0V/15V command input logic
- 0V/15V status output logic
- Minimum pulse suppression (optional)
- Direct or Half-Bridge mode selection
- Adjustable blocking time
- 15V supply voltage
- Single PCB solution with soldered-in gate driver core

Intellectual Property Licensing

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Application Conditions

The design is proposed for the following application conditions:

- General purpose applications and IGBT power modules
- Maximum DC-link voltage of 2200V under switching conditions
- Maximum DC-link voltage of 2850V under non-switching conditions (limited to a duration of 60s)
- Adaptations such as adjustment of gate resistors
Design Description

In addition to the following design description, reference to the datasheet(s) and application manual of the 2SC0535T gate driver family is recommended.

Gate Resistors

Gate resistor values are not explicitly given as they depend on the IGBT power module used and on the application. Gate resistors of either SMD (size 1206) or THT (size PR03) package can be selected.

Turn-on gate resistors:

<table>
<thead>
<tr>
<th>Channel</th>
<th>SMD Package</th>
<th>THT Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>R131a...R131l</td>
<td>R129a, R129b</td>
</tr>
<tr>
<td>2</td>
<td>R231a...R231l</td>
<td>R229a, R229b</td>
</tr>
</tbody>
</table>

Turn-off gate resistors:

<table>
<thead>
<tr>
<th>Channel</th>
<th>SMD Package</th>
<th>THT Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>R130a...R130l</td>
<td>R128a, R128b</td>
</tr>
<tr>
<td>2</td>
<td>R230a...R230l</td>
<td>R228a, R228b</td>
</tr>
</tbody>
</table>

The gate resistors must be determined and assembled by the user. Minimum required gate resistor values are defined in the datasheet of the gate driver 2SC0535T.

V_{CEsat} Monitoring

2SC0535T gate drivers from Power Integrations provide sense inputs for monitoring IGBT short-circuit conditions. In the schematic and bill of material, the resistor networks of the V_{CEsat} monitoring function (R107...R126 and R207...R226) are set for 3.3kV IGBT modules operating at a maximum DC-link voltage of 2200V under switching conditions.

Depending on the actual application conditions and used IGBT power module the following components need to be adjusted (details and calculation methods are described in the corresponding application manual of the gate driver 2SC0535T):

- Capacitors Cax (C101 and C201)
- Resistors Rax (R105 and R205)
- Resistors Rdivx (R106 and R206)
- Capacitors Cvcex (C102...C111 and C202...C211)

Soft Shut Down (SSD)

For this design proposal no dedicated Soft Shut Down function is implemented. Instead, for over voltage protection Dynamic Advanced Active Clamping is implemented.

Dynamic Advanced Active Clamping

Active clamping is a technique designed to partially turn on the IGBT in case the collector-emitter voltage exceeds a predefined threshold. The IGBT is then kept in linear operation. Basic active clamping topologies
implement a single feedback path from the IGBT’s collector through transient voltage suppressor (TVS) diodes to the IGBT gate. This design proposal supports Power Integrations’ Dynamic Advanced Active Clamping (DA²C) based on this principle:

When active clamping is activated, the turn-off MOSFET of the gate driver 2SC0535T is switched off in order to improve the effectiveness of the active clamping and to reduce the losses in the TVS diodes. This feature – called Advanced Active Clamping – is mainly integrated in the secondary-side ASIC of gate driver core 2SC0535T.

Additional TVS diodes have been added in series to the TVS diodes required to withstand the maximum DC voltage under switching operation. These TVS diodes are short-circuited during the IGBT on state as well as for about 15...20µs after the turn-off command to guarantee efficient active clamping. After this delay, these additional TVS diodes are activated and allow the DC-link voltage to be increased to a higher value during the IGBT off-state. This feature – together with Advanced Active Clamping – is called Dynamic Advanced Active Clamping (DA²C). Note that the time during which the voltage can be applied above the value for switching operation should be limited to short periods (<60s).

Minimum Pulse Suppression

This design possesses the option to implement a minimum pulse suppression with a time constant $\tau$. If required the minimum pulse suppression can be set by adjusting C304 and C305. The time constant $\tau$ is given by the following equations:

$$\tau_1 = 0.88k\Omega \cdot C304$$

$$\tau_2 = 0.88k\Omega \cdot C305$$

Recommended values of C304 and C305 are in the range of 100pF ($\tau_x = 88$ns) to 470pF ($\tau_x = 414$ns), depending on actual application conditions.

Blocking Time

During the blocking time the gate driver ignores incoming command signals. The blocking time starts once a fault was detected by the gate driver’s secondary side (undervoltage lock-out or a short-circuit event) or when an undervoltage condition ends on the primary side.
The terminal TB allows the default blocking time of typically 99ms (R318) to be reduced by connecting an optional external resistor to GND. The external resistor $R_b$ needs to be equal or larger than 129kΩ to fulfill the following formula:

$$(R_b + 6.8kΩ) \ || \ 150kΩ \leq T_b + 51ms \text{ with } 20ms < T_b < 99ms$$

In case the terminal TB is directly shorted to GND ($R_b = 0Ω$), the blocking time is set to its minimum value as described in the datasheet of the gate driver core 2SC0535T.
## Interfaces

### Electrical Interfaces

#### X300

<table>
<thead>
<tr>
<th>Pin</th>
<th>Designation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VDC</td>
<td>15V supply (referenced to GND)</td>
</tr>
<tr>
<td>3</td>
<td>VDC</td>
<td>15V supply (referenced to GND)</td>
</tr>
<tr>
<td>5</td>
<td>VCC</td>
<td>15V supply (referenced to GND)</td>
</tr>
<tr>
<td>7</td>
<td>VCC</td>
<td>15V supply (referenced to GND)</td>
</tr>
<tr>
<td>9</td>
<td>SO2</td>
<td>Status output channel 2</td>
</tr>
<tr>
<td>11</td>
<td>INB</td>
<td>Command input channel 2</td>
</tr>
<tr>
<td>13</td>
<td>SO1</td>
<td>Status output channel 1</td>
</tr>
<tr>
<td>15</td>
<td>INA</td>
<td>Command input channel 1</td>
</tr>
<tr>
<td>17</td>
<td>MOD</td>
<td>Mode selector</td>
</tr>
<tr>
<td>19</td>
<td>TB</td>
<td>Set blocking time</td>
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#### X300

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<th>Pin</th>
<th>Designation</th>
<th>Description</th>
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<tbody>
<tr>
<td>2</td>
<td>GND</td>
<td>Ground</td>
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<tr>
<td>4</td>
<td>GND</td>
<td>Ground</td>
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<tr>
<td>6</td>
<td>GND</td>
<td>Ground</td>
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<tr>
<td>8</td>
<td>GND</td>
<td>Ground</td>
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<tr>
<td>10</td>
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<td>Ground</td>
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<tr>
<td>12</td>
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<tr>
<td>14</td>
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<td>18</td>
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#### X100

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<tr>
<td>1</td>
<td>VE1</td>
<td>Emitter channel 1</td>
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<td>2</td>
<td>G1</td>
<td>Gate channel 1</td>
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#### X101

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<tr>
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<td>Collector channel 1</td>
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<tr>
<td>2</td>
<td>C1</td>
<td>Collector channel 1</td>
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#### X200

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<td>Gate channel 2</td>
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<tr>
<td>2</td>
<td>VE2</td>
<td>Emitter channel 2</td>
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#### X201

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<tbody>
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<td>Collector channel 2</td>
</tr>
<tr>
<td>2</td>
<td>C2</td>
<td>Collector channel 2</td>
</tr>
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</table>
The set of CAD data, which includes the circuit schematics, Gerber files, BOM and Pick-and-Place file are available as separate documents bundled together with this documentation.

Layout Example

An example for a suitable layout is shown in the following picture. The recommended PCB thickness is 2.0mm.
### Switching Characteristic

#### Turn-On/Off

The measurement examples shown with the IGBT power modules FZ1500R33HE3 from Infineon Technologies ($R_{\text{Gon}} = 1.0\Omega$ and $R_{\text{Goff}} = 1.5\Omega$) were carried out in a double-pulse test using a half-bridge topology setup at room temperature with an initial DC-link voltage of $2200V_{\text{DC}}$. The adjusted load current is either $1500\text{A (I}_{\text{nom}}\text{)}$ or $3000\text{A (2x I}_{\text{nom}}\text{)}$.

Channel assignment:

- **Channel C2**: Collector current ($1\text{V} \triangleq 1\text{A}$)
- **Channel C3**: Collector-emitter voltage
- **Channel C4**: Gate-emitter voltage

![Graphs showing Turn-On and Turn-Off characteristics](image-url)
**Dynamic Advanced Active Clamping**

The measurement examples shown with the IGBT power modules FZ1500R33HE3 from Infineon Technologies ($R_{\text{on}} = 1.0\,\Omega$ and $R_{\text{off}} = 1.5\,\Omega$) were carried out in a double-pulse test using a half-bridge topology setup at room temperature with an initial DC-link voltage of $2850\,\text{V}_{\text{DC}}$. The load current was set to low levels.

The purpose of these measurements is to demonstrate the effectiveness of Dynamic Advanced Active Clamping in case of DC-link voltages exceeding $2200\,\text{V}_{\text{DC}}$. In the actual application no switching at DC-link voltage exceeding $2200\,\text{V}_{\text{DC}}$ shall be permitted. Non-switching operation up to $2850\,\text{V}_{\text{DC}}$, however, for up to 60s is permitted.

Channel assignment:

- **Channel C2:** Collector current ($1\,\text{V} \triangleq 1\,\text{A}$)
- **Channel C3:** Collector-emitter voltage
- **Channel C4:** Gate-emitter voltage

**Turn-on/off bottom side (single pulse)**

**Turn-on/off bottom side (five pulses consecutively)**
Short-Circuit

The measurement example shown with the IGBT power module FZ1500R33HE3 from Infineon Technologies ($R_{Gon} = 1.0\,\Omega$ and $R_{Goff} = 1.5\,\Omega$) was carried out at room temperature with an initial DC-link voltage of 2200VDC.

Channel assignment:

Channel C1: Status output signal
Channel C2: Collector current (1V $\equiv$ 1A)
Channel C3: Collector-emitter voltage
Channel C4: Gate-emitter voltage

Bottom side
Handling

To avoid possible failures caused by ESD, a handling- and assembly-process with persistent ESD protection is necessary /3/.

References

/1/ 2SC0535T2xx-33 Data Sheet, Power Integrations
/2/ 2SC0535T2xx-33 Description & Application Manual, Power Integrations
/3/ Application Note AN-0902, “Avoiding ESD with CONCEPT Drivers”, Power Integrations

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