Speed and Precision in Gate Drives

High-power gate driver controls MOSFET switches up to 500kHz

Modern power semiconductors allow switching schemes that would have been unthinkable even ten years ago. Conventional MOSFETs, COOLMOS™ devices and prospective compound semiconductor switches are constantly pushing the limits of power density and switching frequency. Only a dedicated gate driver allows the full potential of today's most advanced power switches to be exploited.

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It is common wisdom that prediction is difficult, especially about the future. At the moment, however, it seems as if a multitude of long-cherished dreams are on the point of coming true for designers of power conversion systems. There is great public interest in renewable energy, the concepts of zero emission vehicles and hybrid cars are finally gaining momentum and a whole wave of small improvements to the ecologic footprint of our lifestyle constantly feeds people's awareness of formerly elusive issues such as sustainability and efficiency. All this leverages the role of power electronics, since electricity is the most valuable and flexible form of energy. With that in mind, efficiency is probably the single most important criterion for judging the quality of future energy systems, because no user will accept wasting precious and expensive energy.

MOS Power Switches

MOS switches hold a decisive low-voltage advantage over bipolar devices such as GTOs or IGBTs: their voltage drop under load is determined solely by their turn-on resistance RDS_on. In contrast, IGBTs require a minimum forward voltage drop of several hundred millivolts in order to forward-bias the internal diode. This voltage offset sets an efficiency limit under light load conditions, when only a small current is flowing through the power switch. Whenever the mission profile of the power application includes light-load operation, MOS devices are often the best choice. This opens up a broad range of target systems such as converters for solar panels, auxiliary drives in industry and traction, mains-operated chargers and many more.

High-frequency systems are another typical application area for MOS-gated transistors. The switching losses of bipolar devices increase sharply with operating frequency, because the electron-hole plasma has to be removed and built up in every switching cycle. MOSFETs do not exhibit this high-frequency limitation and can be operated up to several hundred kilohertz and beyond. The main benefits of elevated switching frequency are: smaller systems that occupy less compartment volume, higher power density, a smooth output current waveform, and satisfying functional requirements such as the penetration depth and power coupling in inductive heating systems.

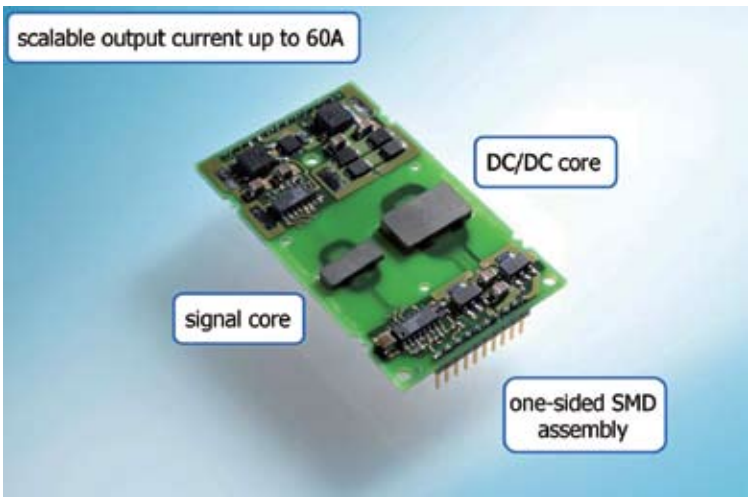

Figure1: Gate driver core 1SC2060P with planar transformers (dimensions 74mm x 44mm x 6.5mm).

Of course there is a fundamental drawback to MOS switches as well - their blocking capability is limited by the comparatively low breakdown

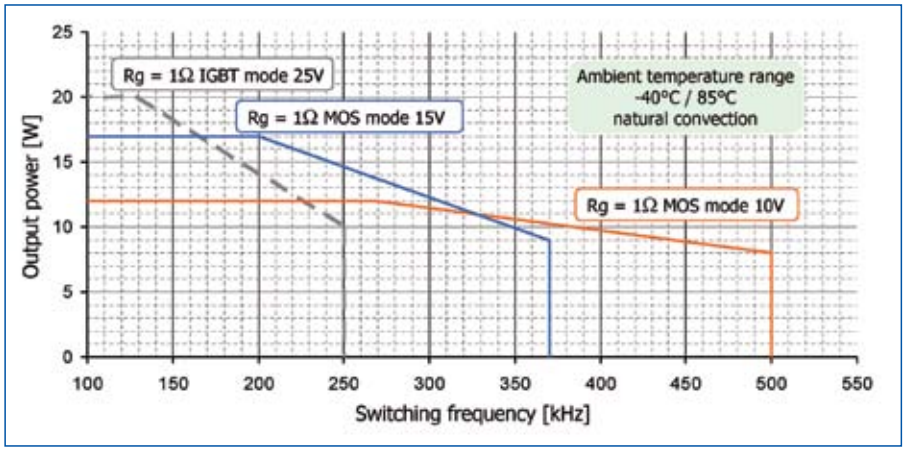

Figure2: Output power vs. switching frequency.

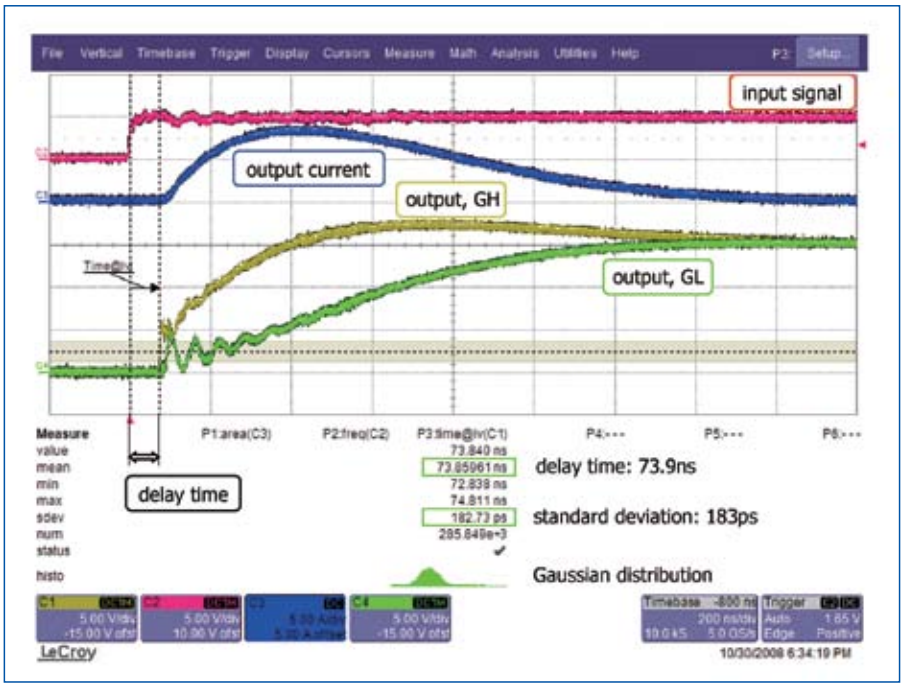

Figure3: Measurement of driver delay and delay time jitter.

field strength of silicon. Typical voltage ratings for conventional power MOSFETs are in the range of 20V to 300V. Charge compensation devices, such as COOLMOS™, can break this barrier with blocking voltages of up to 600V and even 900V.

An alternative approach has been followed for more than two decades. If the properties of silicon are limiting, why not use another material? SiC, GaN and a great variety of other compound semiconductors offer superior features such as breakdown field strength and thermal conductivity. The time might finally have come for these new power devices after a long maturing process and constant cost-performance improvements.

High-Frequency Gate Driver

No matter which device type is used in a given application, the main current and thus the power flux is determined by the charging and discharging process of the device's gate capacitance. The required drive power is supplied by a high-performance gate driver such as the 1SC2060P shown in Fig. 1. A dedicated MOSFET mode is implemented in the 1SC2060P. It allows the optimum output voltage swing Vdd across the power switch to be chosen freely. Any value between 10V and 20V can be utilized, whereas the separate IGBT mode incorporates switching up to 25V (–10V / +15V). The driver shown in Fig. 1 is based on CONCEPT's recently introduced SCALE-2 ASIC chipset. Full

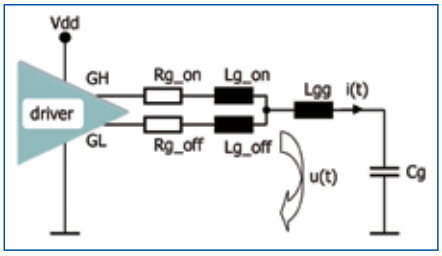

Figure4: Circuit representation of a typical gate loop (simplified).

custom integration of almost all gate driver functions into ICs leads to an enormous 80% reduction in component count compared to conventional solutions.

Figure 2 shows the output power versus the switching frequency of the gate driver. The gate resistance is 1.0W for both the turn-on and turn-off resistors. The maximum switching frequency is limited by the self-heating of the driver under natural convection cooling. In MOS mode, the driver allows extremely fast switching of up to 500kHz for an output voltage swing of 10V and 370kHz for one of 15V. The output curve in IGBT mode is shown for comparison. Dedicated thermal balancing trades a part of the 20W in IGBT mode off against a higher switching frequency in MOS mode.

Gate Control

Fast switching in the hundreds of kilohertz range not only requires high drive power and maximum frequency but also tight control over crucial parameters such as the driver's delay time and the associated jitter. A fast driver with a short delay introduces significantly less phase lag into the power system's control loop. Less phase lag is of great importance for maintaining the stability of the control loop, thus allowing the benefits of fast switching to be fully exploited. Fig. 3 shows the measurement of driver delay and delay time jitter. The graph reveals ultra-fast switching at a typical 74ns delay and enormous reproducibility with a standard deviation of less than 185ps. The total delay variation is virtually negligible with a maximum of ±1ns over 285,000 acquisitions. This combination of power and precision makes the 1SC2060P the first choice for highly optimized systems, where tight control over timing margins is mandatory.

At very high frequency switching, the influence of parasitic circuit elements has to be considered to obtain optimum performance in the gate drive loop. Figure 4 illustrates a simplified gate loop consisting of a driver module, the turn-on and turn-off gate resistors, parasitic inductances of the gate resistors, the parasitic inductance of the power switch gate and an effective load capacitor. This configuration is a well-known standard RLC resonance circuit. For both the turn-on and turn-off transition, the elements can be concentrated into an effective gate resistance Rg, the load capacitance Cg and the sum of all effective parasitic inductances Lg. The gate drive current i(t) is then governed by the differential equation (1).

$$Lg \cdot \frac{d^2 i(t)}{dt^2} + Rg \cdot \frac{di(t)}{dt} + \frac{i}{Cg} = \quad (1)$$

Solving for i(t) yields the time-dependent drive current. Even in the simplest case with constant parameters Lg, Rg, and Cg, the solution shows two distinct characteristics depending on the ratio of the damping resistance Rg to Lg and Cg. If Rg is too low, the current waveform will take the form of a damped harmonic oscillation. This case is undesirable in a gate control loop because it leads to a gradual loss of controllability and because of serious EMC problems. If Rg is very high, slow settling towards the final value will occur without any oscillations. The boundary between these two characteristics is given by equation (2) in our model.

$$Rg \geq 2\sqrt{\frac{Lg}{Cg}} \quad (2)$$

The fastest switching of the power gate can be obtained by letting both sides of equation (2) be equal. The gate current in this critically damped case exhibits the steepest slopes possible for non-oscillating waveforms. It is interesting to note that there is a maximum peak current for which the gate loop remains free of oscillations. The upper limit of that current is given by equation (3).

$$I_{max} = \frac{2}{e} \cdot \frac{Vdd}{Rg} \approx 0.74 \cdot \frac{Vdd}{Rg} \quad (3)$$

In real-life applications, the model from Fig. 4 is too simplistic to model the circuit behavior. The maximum stable peak current is typically lower than the limit of equation (3) and is often close to two thirds of Vdd/Rg. Figure 5 shows an exemplary turn-on transition from 0V to 15V with a 1.0W gate resistor where the peak current only reaches 10A instead of the theoretical maximum of 15A. Thus the 60A current rating of the 1SC2060P leaves ample reserve for even the largest MOSFET power switches.

Figure 5 also shows the acquisition of the gate charge Qg per switching transition. Qg is equivalent to the area under the gate current curve. The required drive power can easily be calculated from equation (4).

$$P_{drv} = f \cdot Vdd \cdot Qg \quad (4)$$

Equation (4) is very simple but still much more precise than the widespread approach of obtaining the required drive power from the datasheet value of the input capacitance. The curve of MOS gate charge versus input voltage is highly non-linear. As a result, only the actual gate charge value Qg can yield a correct prediction about the drive power needed in the given application.

Planar Transformer HV Technology

The 1SC2060P driver core comes with an ultra-flat form factor and measures only 6.5mm in height. This is achieved by using newly developed planar transformer technology. A schematic cross

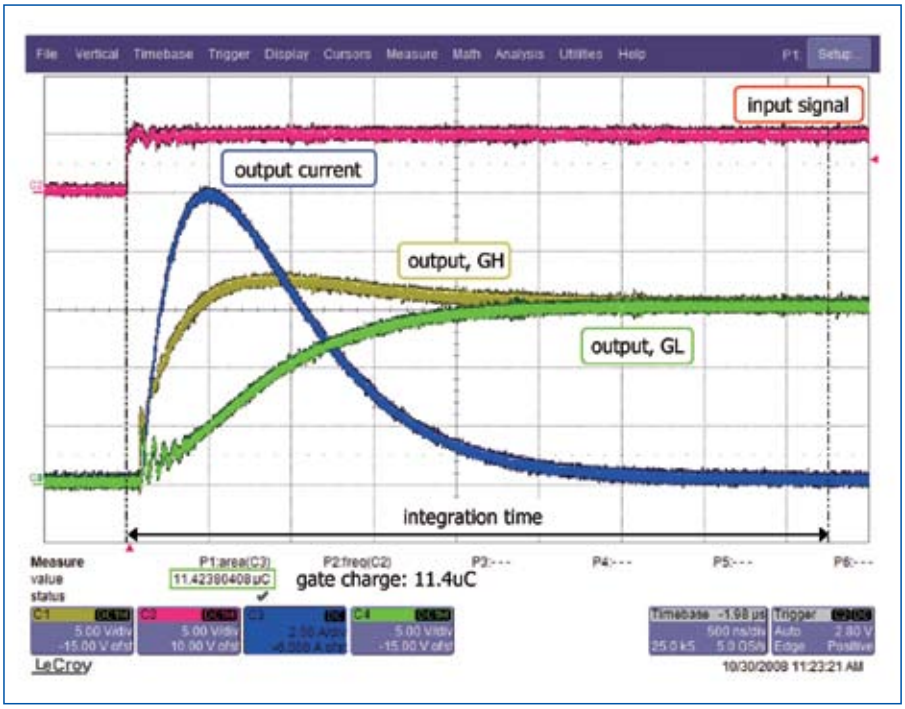

Figure5: Turn-on transition at 1W gate resistance and 15V driving voltage.

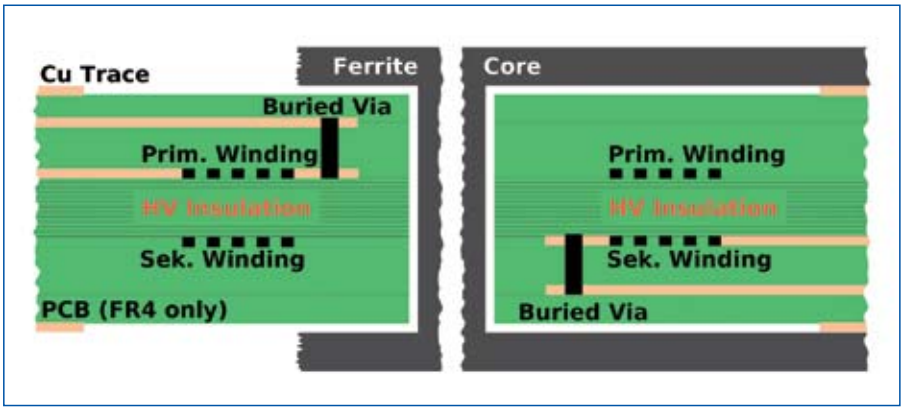

Figure6: Schematic cross section of the HV planar transformer.

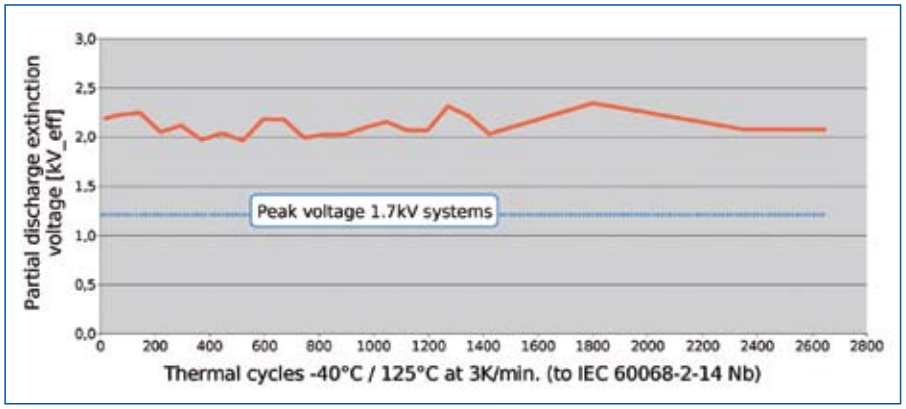

Figure7: Insulation stability versus slow thermal cycling.

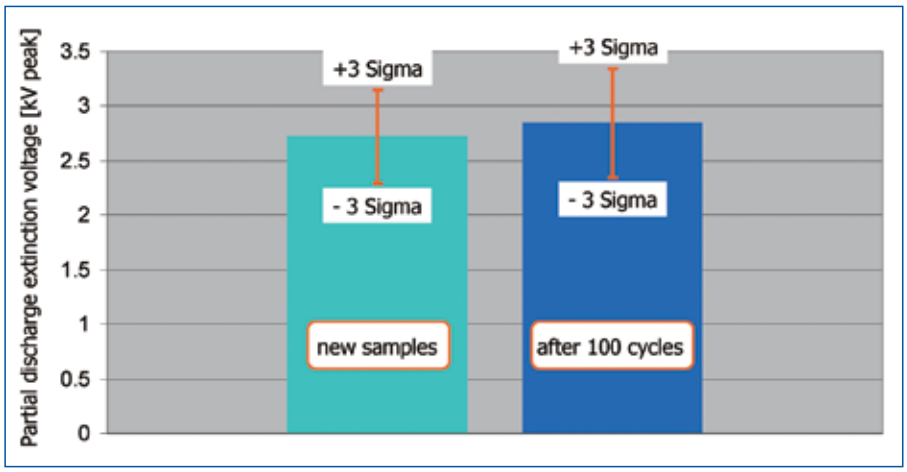

Figure8: Highly accelerated thermal shock testing (-55°C / +150°C to IEC 60068-2-14 Na).

section is shown in Fig. 6, as already reported in PSDE of July 2008. In contrast to common planar designs in low-voltage systems, there is no interleaving of the primary and secondary windings in the layer stack. A dedicated high-voltage insulation layer is placed between the primary and secondary windings with no crossings or vias penetrating it. The specific effect of this construction is an unusually high voltage rating for the insulation of the planar transformer. The 1SC2060P provides galvanic isolation up to 1.7kV – enough even for future generations of MOS switches.

Planar transformers for high-voltage drivers are not only characterized by high power density and cost-effective automated manufacturing, they also excel in high-speed switching due to their low stray inductance.

Reliability

Power systems are generally designed to ensure high availability throughout their lifetime. It is therefore important to make sure that the reliability figures of every component in the power system are much higher than expected from the application, because the failure probabilities of the individual components add up in the system.

One of the greatest contributors to the failure rate is the number of components on the printed circuit board. The 1SC2060P uses the latest SCALE-2 chipset to reduce the component count by 80%. Supporting passive components have been carefully selected for appropriate voltage rating, temperature range and degradation over time.

The high-voltage insulation needs to withstand thousands of thermal cycles, over-voltage peaks, mechanical stress, the influence of humidity and many more parameters. Planar transformers on the printed circuit board benefit from the high stability of fiber-reinforced epoxy that has proved to maintain its characteristics in the field. Figure 7 shows the results of accelerated life testing with slow thermal cycles. The partial discharge extinction voltage is the most sensitive and dependable criterion of insulation performance. No degradation is visible after as many as 2,600 cycles. This accumulated stress is equivalent to more than 20 years under real-life application conditions. Exorbitantly harsh thermal shock cycles between –55°C and +150°C have been applied to probe even further. Again, virtually no change in insulation characteristics can be seen, as evidenced in Fig. 8. The tight 3-sigma boundaries of the partial discharge extinction voltage shown in Fig. 8 highlight the stable uniformity of the planar insulation.

Numerous additional tests have been performed to assess the aging behavior of the planar transformers. Mechanical shock tests up to 2000m/s^2 showed absolutely no impact on mechanical or electrical parameters. The effect of humidity has been investigated by temperature, humidity and bias testing at 85°C, 85% RH and a constant DC bias of 1500V. No failures occurred after more than 1000 hours in this truly extreme climate.

Summary

A dedicated high-frequency gate driver is needed to fully exploit the capabilities of state-of-the-art MOS power devices. The 1SC2060P driver core has been specifically designed for high-power and ultra-fast switching to satisfy this need. It employs SCALE-2 chipset technology and newly developed planar transformers for unrivalled timing precision, high power density and an attractive flat form factor. The 500kHz gate drive module has been extensively tested for performance and reliability under harsh environmental conditions.

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