Application of Gate Drivers for 3-Level NPC-2 Power Modules with Reverse Blocking IGBTs

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Abstract

3-level topologies have been widely used in various applications for several years. Such applications are typically based on the classical neutral-point-clamped (NPC1) topology with four power switches (IGBT) per half-bridge and two additional clamping diodes. A variant of this topology is known as the NPC2 topology which uses two IGBTs per half-bridge and two IGBTs connected as a common collector configuration in the clamping path. This topology is also available with two reverse blocking (RB) IGBTs instead of IGBTs in a common collector configuration to reduce the amount of conducting components. The gate driver requirements – especially concerning protection functions like desaturation monitoring and active clamping – are different for NPC1/NPC2 and NPC2 with RB-IGBT topology. This paper discusses these differences and provides proven solutions that enable standard gate drivers to be adapted for use in NPC2 topology designs with RB-IGBTs.

1 Introduction

Conventional 2-level converter topologies (Fig. 1a) feature two switching states; the positive and negative rail of the DC-link voltage (DC+, DC-). To reduce total harmonic distortion in the output waveforms, further switching states are desired. The well-known 3-level NPC1 topology (Fig. 1b) provides such an additional switching state, the neutral state of 0V of junction N. Due to the lower voltage waveform distortions, filtering requirements can be reduced. This makes these topologies more and more attractive as the cost of filters has become a significant factor in the design of converter systems. A drawback of implementing 3-level topologies is the increased amount of switching devices (IGBTs and diodes), which add to the complexity and also partially to the cost of the entire system [1]. With the implementation of the NPC2 topology (Fig. 1c) the amount of power semiconductors can be further reduced, compared to the classical NPC1 setup.

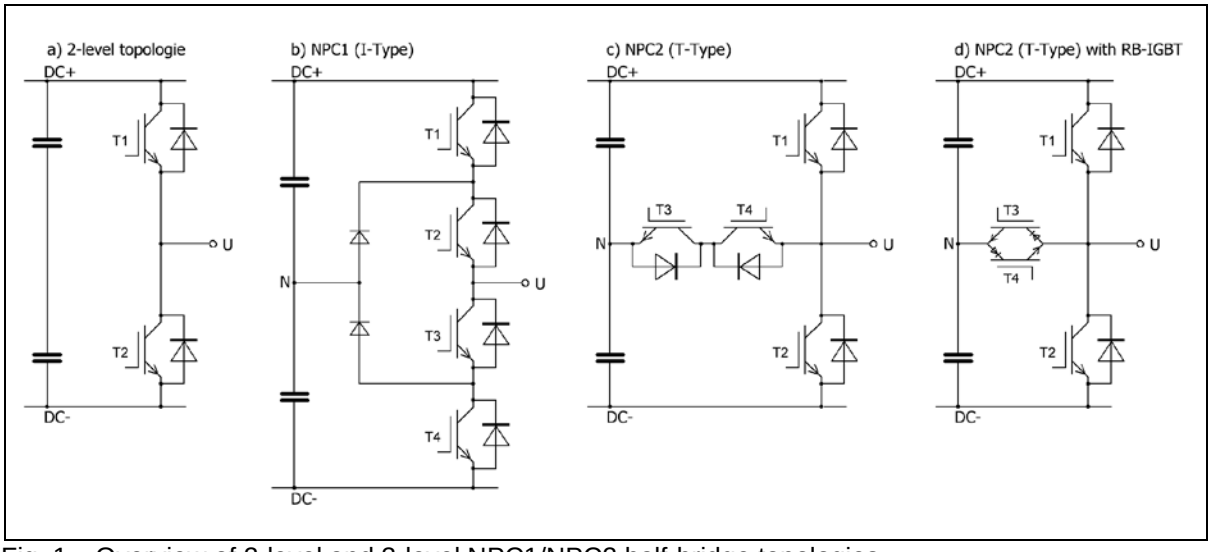

Fig. 1 Overview of 2-level and 3-level NPC1/NPC2 half-bridge topologies

Instead of two IGBTs and diodes, which are connected as a common collector topology in NPC2 setups, two reverse-blocking (RB) IGBTs can be used. RB-IGBTs possess an altered internal structure, which enables the IGBT to sustain forward and reversed biased voltages of equal levels. In comparison, in the reverse blocking state a standard IGBT sustains only a fraction of the forward blocking voltage. Therefore, RB-IGBTs mean that NPC2 topology designs can be implemented using two fewer diodes (Fig. 1d). This leads to several advantages including reduced conduction losses, better utilization of package area, simplified auxiliary terminal arrangement of the power module and others [2].

2 Gate driver considerations

The requirements for the IGBT gate driver differ for the topologies presented in Fig. 1. For instance, a 2-level topology typically requires features such as short-circuit and overvoltage protection. A widely-used implementation of the short-circuit protection is called V_{CEsat} or desaturation monitoring, shown in the Fig. 6. Overvoltage protection is commonly achieved using active clamping of the IGBT's collector-emitter voltage. Fig. 4a shows an example.

If a 3-level NPC1 topology is used, the turn-off sequence of the IGBTs during a short-circuit event is important. In this case, it is mandatory that first the outer IGBT of a half-bridge is turned-off before the inner IGBT is switched off. If this sequence is not followed, the inner IGBT will be exposed to the full DC-link voltage and will be destroyed as the IGBTs in a 3-level NPC1 topology are "only" rated for half of the DC-link voltage [1]. Accordingly, the gate driver shall not automatically turn-off the IGBTs in the event of short-circuit, but report the fault condition to the control unit, which will ensure the proper turn-off sequence. Only if Advanced Active Clamping is implemented for the inner IGBTs can the turn-off sequence be ignored and the gate driver allowed to turn-off automatically [3].

Common for all the NPC topologies shown in Fig. 1 is that during normal operation the voltage of the phase output U alternates between $^1/_2$DC+ and $^1/_2$DC- with respect to the neutral point N, i.e. it changes its polarity. This fact is of particular interest for the IGBTs between junctions N and U of the NPC2 topology forming the bidirectional switch. The resulting voltages for these IGBTs are shown in Fig. 2 if the outer switches (not illustrated here) are turned on and off respectively.

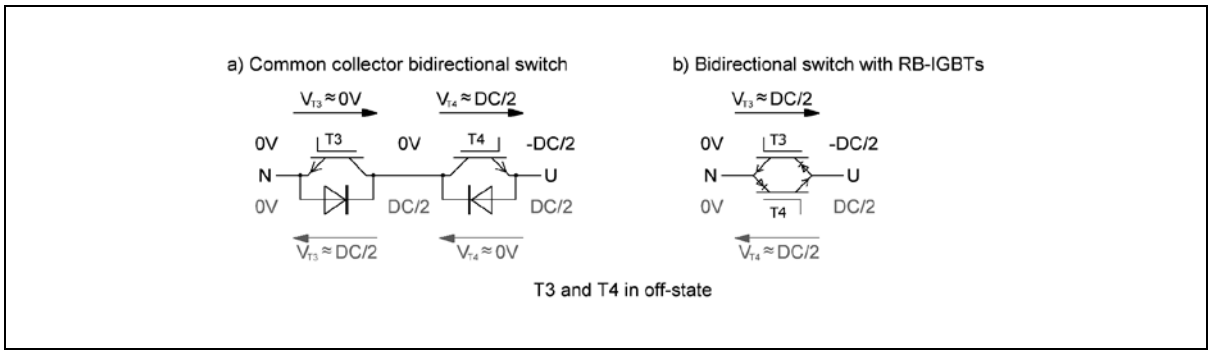

Fig. 2 Idealized voltage distribution for a bidirectional switch

The collector-emitter voltage of the IGBT switches in Fig. 2a is always positive or (idealized) zero; depending of the actual phase output voltage at position U. Hence, for short-circuit and overvoltage protection, no special requirements need to be considered. However, this is different if RB-IGBTs are used as the bidirectional switch, and the alternating voltage at junction U demands modifications of classical short-circuit and overvoltage protection schemes. Otherwise, the gate driver stage and eventually the IGBT switch(es) will be damaged.

As an example, Fig. 3 (left) shows measurements using the NPC2 power module 4MBI650VB-120R1-50 from Fuji Electric. The load in this instance is connected between U and DC-, while the top switch T1 is turned on and turned off. The waveform of channel 2 („VCE RB-IGBT T3") illustrates the alternating voltage between N-U during the turn-on and turn-off phases of IGBT T1.

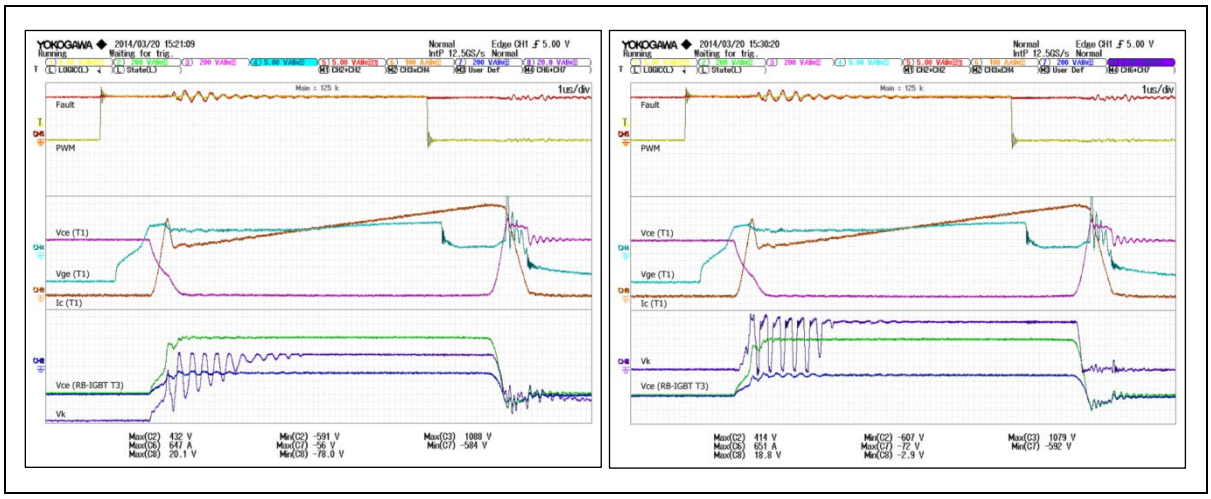

Fig. 3 Switching waveforms of an NPC2 topology with RB-IGBTs (V_{DC} = 800V, I_{load} = 650A)

2.1 Overvoltage protection

To protect IGBTs in general against transient overvoltages during turn-off events, an active clamping circuit is commonly used. (For low power applications alternatives like “two-level turn-off” or “soft-shutdown” may also be used [1]). Overvoltage is caused by the stray inductance within the commutation loop and the change of commutation current ($^{di}/_{dt}$). Active clamping limits the overvoltage reliably, as proven in numerous applications by driving the IGBT into the active region and reducing the $^{di}/_{dt}$.

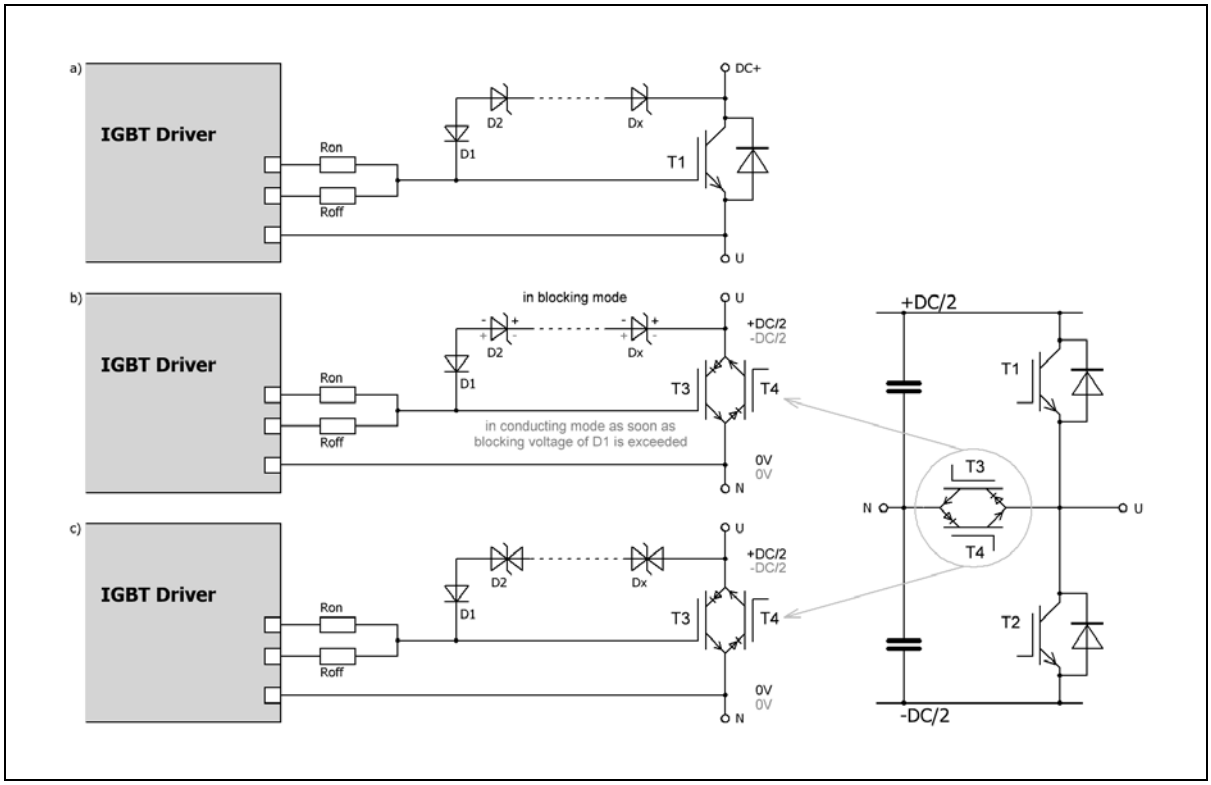

Fig. 4 Active clamping circuit for a) standard IGBTs and b), c) RB-IGBTs

A standard active clamping setup is shown in Fig. 4a for IGBT T1. The TVS diodes (D2…Dx) are selected according to the actual application conditions (e.g. DC-link voltage, V_{CES}-class of the IGBT) and are connected from the collector to the gate via a low-voltage Schottky diode or PIN diode (D1). This diode is necessary to avoid a current flow from the gate into the IGBT collector, and requires only a blocking capability of, for example, 40V. However, if an NPC2

topology with RB-IGBTs is selected, the typical active clamping circuit with unidirectional TVS diodes and a low-voltage diode cannot be used. This is because the voltage across the RB-IGBTs will change the polarity depending on the switching states (Fig. 4b). As long as the polarity of the collector of the respective IGBT is positive, the TVS diodes of the corresponding gate driver can block this voltage from the driver. However, as soon as the collector voltage reverses its polarity the TVS diodes start to conduct and the full collector potential will be applied to the anode of low-voltage diode D1. This voltage is approximately equal to half of the DC-link voltage, and would lead to the destruction of the IGBT driver and the associated IGBT.

As a counter measure, there are two possible options. For the first solution one must use bidirectional instead of unidirectional TVS diodes as shown in Fig. 4c. The drawback, however, as visible in Fig. 3, is that the negative voltage “Max(C2)” may reach levels which are equal to the break-down voltage of the bidirectional TVS diodes. This will still result in a too high reverse voltage of the diode D1. Therefore, this approach is not recommended.

The second and preferred solution is easily realized by replacing the low-voltage diode D1 with a high voltage diode. This high voltage diode must have a blocking capability of at least half the DC-link voltage. Note, that besides the blocking voltage, the creepage and clearance distances of the diode must also be considered. In some cases it may be necessary to use more than one diode.

2.1.1 Advanced Active Clamping

To increase the efficiency of the active clamping circuit, CONCEPT implemented in several of its gate drivers the so-called Advanced Active Clamping (AAC) function. AAC uses an additional feedback path at the internal gate driver output stage. Depending on the actual clamping current/overvoltage condition, the internal output stage MOSFET will be switched off progressively [4].

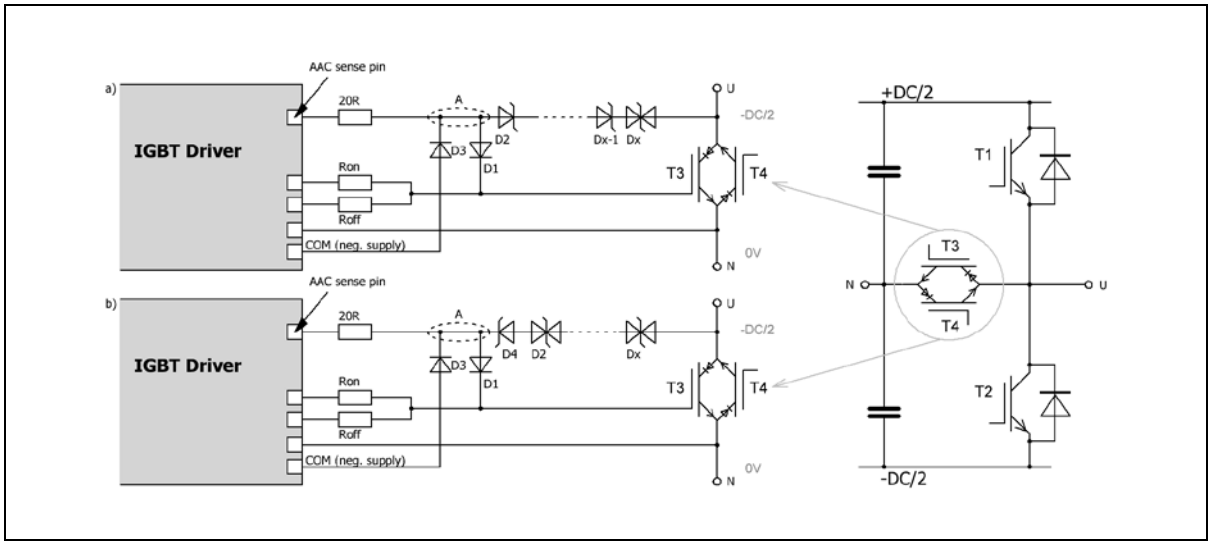

Fig. 5 Advanced Active clamping circuit for a) standard IGBTs and b) RB-IGBTs

Using the NPC2 topology with RB-IGBTs requires a modification of the usual AAC design. Fig. 5a shows the widely-used AAC circuit for standard IGBTs with D1 and D3 (low voltage diodes). As only one bi-directional TVS diode is used (Dx), a dangerously high voltage will establish itself at junction A when –DC/2 is applied at terminal U. This will lead to an overload of diodes D1 and D3 and the 20R resistor, and eventually of the entire gate driver stage. To prevent this high voltage occurring, it is recommended that all uni-directional TVS diodes are substituted with bi-directional devices. In addition, a further uni-directional TVS diode D4 needs to be placed in series with those diodes (Fig. 5b). The now asymmetrical break-down voltage of the TVS diode network ensures that the established voltage at junction A is within safe range when the negative voltage (-DC/2) is present at the phase output, while the operation in forward direction with positive voltage (DC/2) is working as usual (assuming that

the TVS diodes are selected in accordance to the actual application conditions).

2.2 Short-circuit protection

To protect IGBTs of any topology during a short-circuit event, a reliable desaturation monitoring function is required. A widely-used implementation of desaturation monitoring with high-voltage diodes is shown in Fig. 6. This setup is typically used to detect a short-circuit. A more advanced solution is to replace the high voltage diodes with a resistor network (R_{vce} in Fig. 7a), which allows the V_{CE} voltage to be measured during the IGBT turn-on state. This avoids inadvertent tripping of the monitoring function [1]. Both implementations can be used for 2-level and 3-level NPC1/NPC2 topologies.

However, if NPC2 topology with RB-IGBTs is preferred, the desaturation monitoring with high-voltage diodes method will not work anymore. For the same reasons that were explained for the overvoltage protection, this approach will work for as long as the corresponding collector voltage has positive potential (referenced to the emitter) and the high voltage diodes of the corresponding gate driver can block this voltage from the driver's low voltage sense input. But once the polarity turns negative, the diodes start to conduct and an excessive current will flow through the diodes, which will damage the driver and/or associated IGBT.

By implementing short-circuit protection using a resistor network, the resistors R_{vce} scale down the collector voltage as well as limiting the current flowing from the collector to the gate driver sense input. The next section of this paper briefly describes the principle of this circuitry. [5].

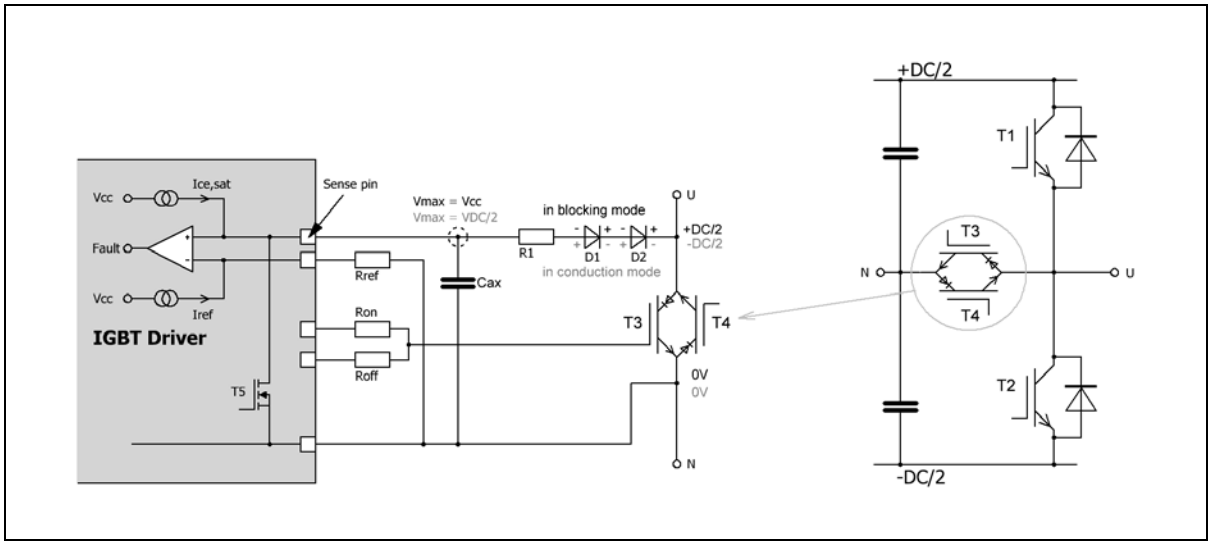

Fig. 6 Desaturation monitoring with high-voltage diodes

2.2.1 Short-circuit protection with resistor network

The following explanation references Fig. 7. During an IGBT off-state, the driver's internal MOSFET connects the sense pin to COM (negative potential of the gate driver). The capacitor C_{ax} is then pre-charged/discharged to the negative supply voltage. Without diode D1, a voltage V_K will establish itself at junction K, which can be calculated according to Eq. 1.

Eq. 1 $$\boldsymbol{V_K = V_{CE,max} \cdot \frac{R_{ax}}{R_{ax} + R_{VCE}}}$$

The function of D1 is to clamp the voltage V_K to the positive supply voltage V_{CC} to protect the sense input of the gate driver against high voltages. The maximum current flowing into junction K can be calculated according to the following formula:

Eq. 2 $$\boldsymbol{I_{vce} = \frac{V_{CE} - V_{CC}}{R_{VCE}}}$$

To limit the losses in the resistor network and diode D1 it is recommended to adjust the current to 0.6…1mA at maximum DC-link voltage.

The current flowing into junction F can be calculated according to Eq. 3. This current will flow during the on-state and charges C_{ax}. The time required to charge C_{ax} determines the response time of the short-circuit protection.

Eq. 3 $$\boldsymbol{I_{ax} = \frac{V_{CC}}{R_{ax}}}$$

At IGBT turn-on and in the on-state the above mentioned MOSFET turns-off. While V_{CE} decreases, C_{ax} is charged from the COM potential to the IGBT saturation voltage. The voltage of C_{ax} is constantly compared with a reference voltage determined by R_{ref}. In the event of a short-circuit, the voltage of capacitor C_{ax} increases as the IGBT is driven out of the saturation. Once the voltage of C_{ax} is higher than the reference voltage, the gate driver will interpret this as a fault condition. Fig. 7b illustrates this scenario.

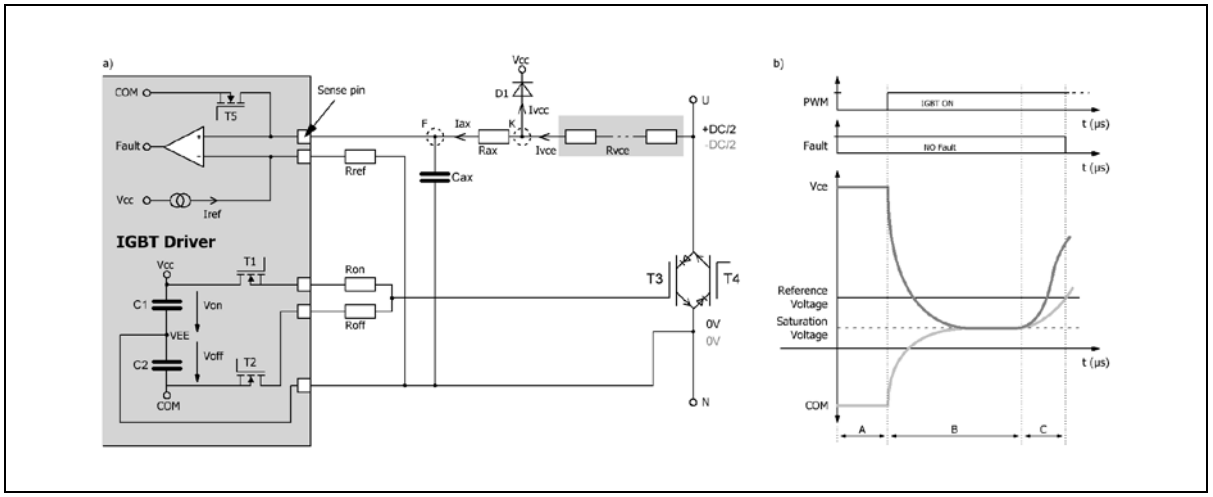

Fig. 7 Schematic of desaturation monitoring using resistor network

If a negative voltage is present during the off-state, the voltage a junction K will also be negative. To prevent a current flow out of the sense pin of the gate driver it is necessary to add a further diode D2 to the circuitry (Fig. 8). Otherwise, substrate currents and unintended latch-up effects will occur within the gate drive circuitry note: it is also possible to implement active rectification inside the ASIC to address this point). Diode D2 clamps the junction K to the emitter potential, preventing/limiting any current flow out of the sense pin of the gate driver.

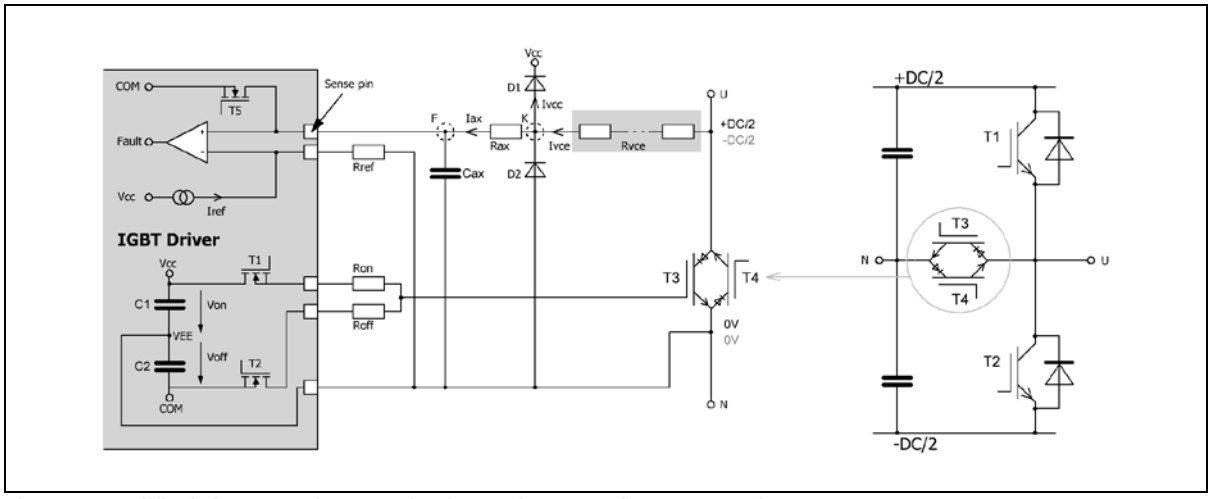

Fig. 8 Modified desaturation monitoring using a resistor network

Fig. 9 illustrates the successful short-circuit handling capability of Fuji Electric's RB-IGBT NPC2 4MBI300VG-120R-50 power module used together with an off-the-shelf 2SC0106T core gate driver from CONCEPT (other core gate driver like 2SC0108T and 2SC0435T are also suitable) and the proposed short-circuit and active clamping modifications. The applied DC-link voltage is 800V using a standard setup without snubber capacitors.

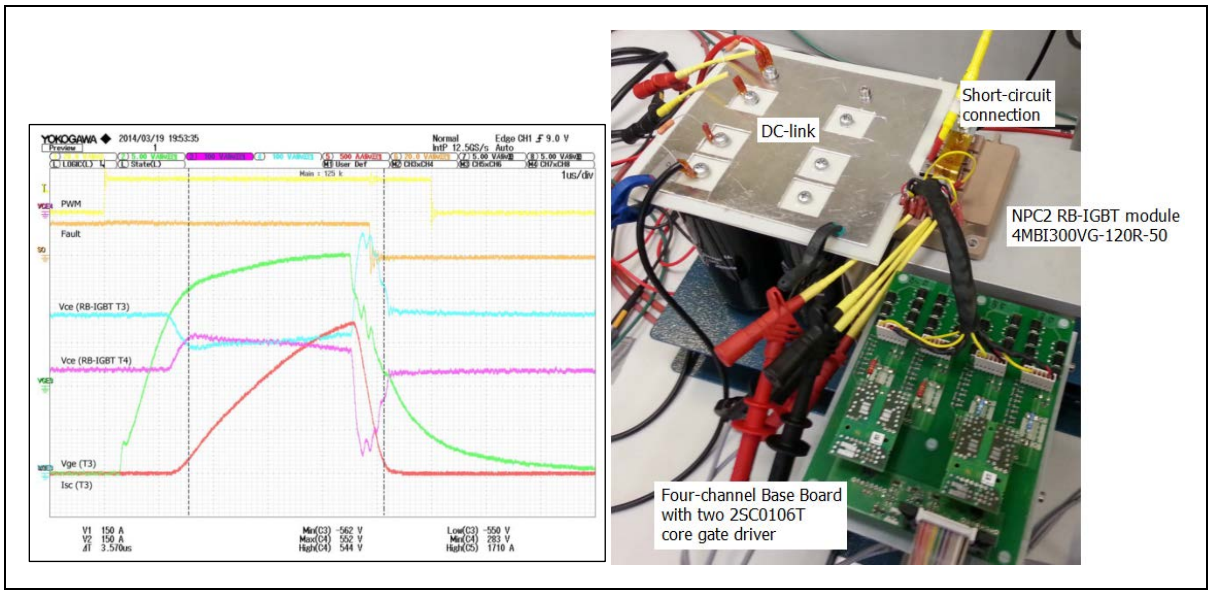

Fig. 9 Short-circuit test with the proposed gate driver modifications

3 Conclusion

As demonstrated, for NPC2 topologies using RB-IGBTs it is necessary to make modifications to classical protection functions like desaturation monitoring and collector-emitter clamping of a gate driver. These modifications can be easily implemented using standard gate driver cores from CONCEPT. Without these modifications the gate driver and eventually the entire power stage will be damaged as the negative voltage at the phase output will overload the gate driver unit. The proposed solutions open the way for the new technology of RB-IGBTs in applications like solar power and UPS.

4 Reference

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[7] Datasheet, "4MBI300VG-120R-50", Fuji Electric

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