Application Note AN-83
BridgeSwitch Family

BridgeSwitch Tips, Techniques and Troubleshooting Guide

Introduction

The BridgeSwitch™ family of integrated half-bridges dramatically simplifies the development and production of high-voltage inverter driven 2- or 3-phase PM or BLDC motor drives. It incorporates two high-voltage N-channel power FREDFETs with low and high-side drivers in a single small-outline package. The internal power FREDFETs offer ultra-soft and ultrafast diodes ideally suited for hard switched inverter drives. Both drivers are self-supplied eliminating the need for an external auxiliary power supply. BridgeSwitch provides a unique instantaneous phase current output signal simplifying implementation of sensor-less control schemes. The low-profile, compact footprint surface mount package offers extended creepage distances and allows heat sinking of both power FREDFETs through the printed circuit board.

BridgeSwitch offers internal fault protection functions and external system level monitoring. Internal fault protection includes cycle-by-cycle current limit for both FREDFETs and two level thermal overload protection. External system level monitoring includes DC bus sensing with four undervoltage levels and one overvoltage level as well as driving external sensors such as an NTC. The bi-directional bussed single wire status interface reports observed status changes.

Typical applications include pumps for dishwashers or washing machines, refrigerator compressors, ceiling fans or fans in high efficiency air conditioners.

Scope

The application note provides answers to common BridgeSwitch technical questions, including:

- Optimum Device Placement for Best Thermal Performance
- External Device Supply
- Composite DC Bus Monitoring
- Hardware Based Motor Inrush Current Limiting (soft-start)
- Complementary PWM Signal Operation
- PWM Signal Polarity Inverter for High-side /INH Input
- Inverter Inhibit Function
- Determining Operating Junction and PCB Temperature

A Troubleshooting Guide at the end of the document provides suggestions how to address possible inverter misbehavior.

Other Technical Support Documents

- BridgeSwitch Family Data Sheet
- AN-80: BridgeSwitch FAULT Communication Interface
- UL Informative Report IEC 60335-1 and IEC 60730-1
- DER-653: 300 W 3-phase Inverter Development Platform With BridgeSwitch and LinkSwitch™-TN2
- DER-654: 300 W 3-phase Stand-alone Inverter With BridgeSwitch
- DER-749: 40 W 3-phase Fan Reference Design With BridgeSwitch and LinkSwitch-TN2

All documents are available for download at www.power.com: https://motor-driver.power.com/products/bridgeswitch-family/bridgeswitch/

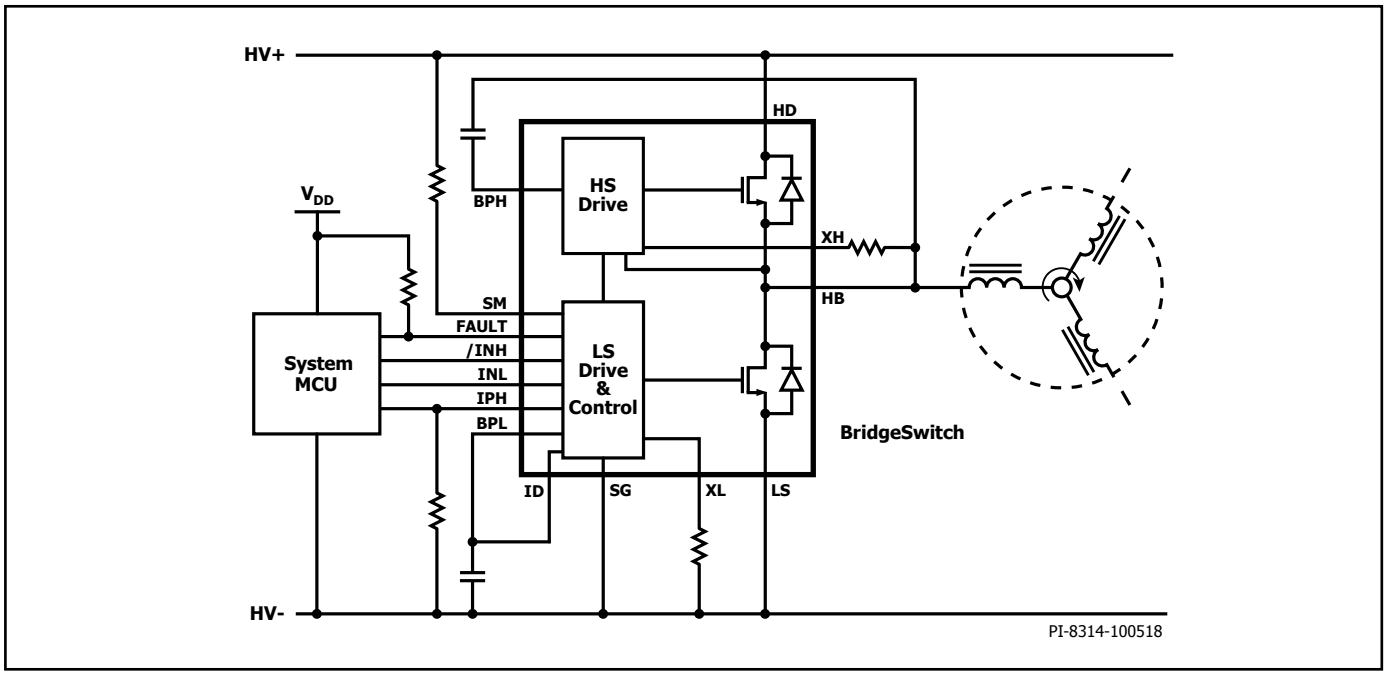


Figure 1. *Typical 3-Phase Inverter Schematic (BRD126X).*

Optimum Device Placement for Best Thermal Performance

PCB layout plays an important role in the thermal performance of 3-phase inverter designs employing BridgeSwitch ICs. Its InSOP-24C package has two exposed pads, which facilitate heat transfer from the power switches to the printed circuit board (PCB). They are marked HD and HB as shown in Figure 2.

The arrangement of the three devices and the distance between them, the size of the copper clad areas connected to the exposed pads, and the thickness of the copper all impact thermal performance. Placing the devices in a triangular configuration can lower device temperature significantly compared to a linear configuration while reducing temperature variation between devices at the same time. The advantage of the triangular configuration becomes more prominent in higher density designs.

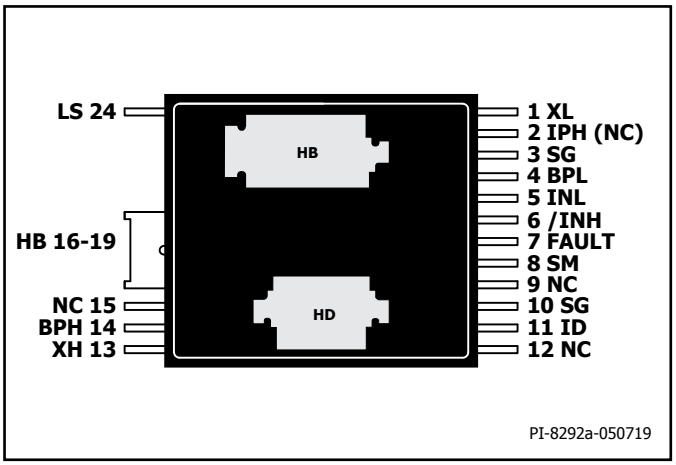


Figure 2. *InSOP-24C (Bottom View).*

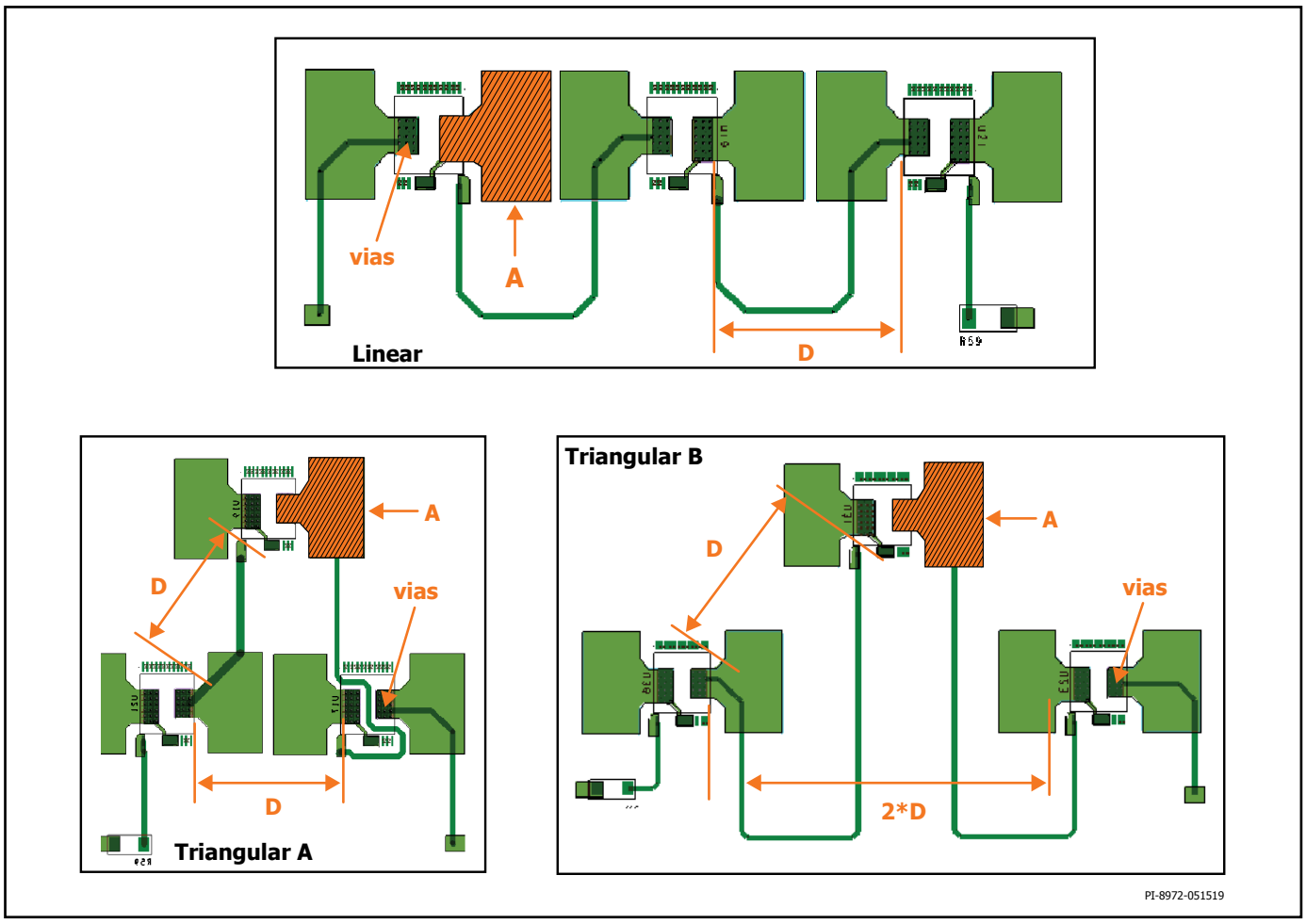


Figure 3. *Linear and Triangular A and B Device Configurations (Bottom Layer).*

Figure 3 depicts three possible device arrangements. The two triangular configurations include an equilateral triangle (Triangular A) or an isosceles triangle (Triangular B). Distance D between devices determines the density of a given layout. Each exposed pad connects to a copper clad area A on the PCB for improved heat transfer.

Figure 4 plots average rise of device temperature above ambient temperature comparing the three different PCB layout configurations (refer to Figure 3) over copper clad area A and device distance D. The PCB material is FR4 laminate with a copper thickness of 70 µm (610 g/m²). It has two layers with a copper clad area A each on both sides for further improved heat transfer. The effective total area is therefore 2 × A. Both layers connect through thermal vias, which reside directly underneath the exposed pads of the InSOP-24C package and have an outer diameter of 0.8 mm and an inner diameter of 0.5 mm. A controlled current forward biases both FREDFET recovery diodes of each BridgeSwitch BRD1265C device to impose a fixed dissipation of 0.75 W per diode. The resulting total package dissipation is 1.5 W

Table 1 summarizes test results with a PCB copper area A = 600 mm² each per layer.

Device Distance D	17 mm	25 mm
Average Temperature Rise Linear Configuration (A = 600 mm²)	63.8 °C	56.9 °C
Average Temperature Rise Triangular A Configuration (A = 600 mm²)	55.1 °C	51.8 °C
Average Temperature Rise Triangular B Configuration (A = 600 mm²)	50.8 °C	48.4 °C

Table 1. *Average Temperature Rise above Ambient Temperature with A = 600 mm² Per Layer Copper Clad Area.*

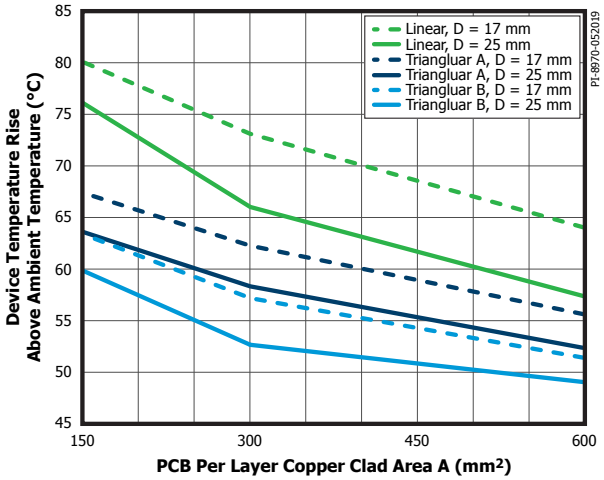
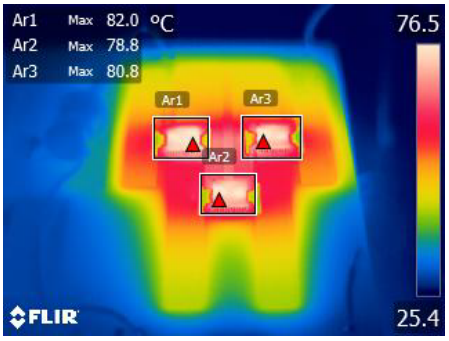


Figure 4. *Average Device Temperature Rise vs. Configuration, Per Layer Copper Clad Area A, and Device Distance D at 1.5 W Package Dissipation.*

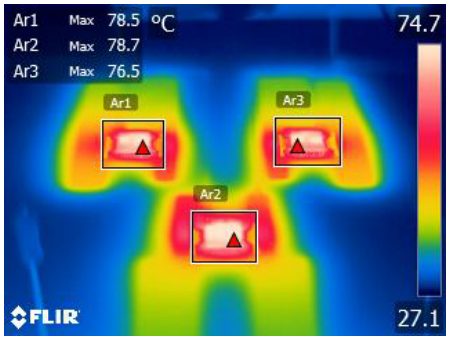
Both triangular configurations reduce significantly average device temperature rise compared to the linear configuration. For a device distance D=25 mm and copper clad area A=600 mm², Triangular A configuration reduces average device temperature rise by 5.1 °C and Triangular B configuration reduces the average temperature rise by 8.5 °C compared to the linear configuration. For a device distance D=17 mm and A=600 mm², the average temperature rise is 8.7 °C lower for Triangular A and 13.0 °C lower for Triangular B, respectively, compared to the linear configuration. Note, that both triangular configurations still have a lower device temperature rise in a more dense design with D=17 mm compared to the linear configuration in a less dense design with a device distance D=25 mm.

Figure 5 depicts thermal device scans for both triangular configurations and the linear configuration with a PCB per layer copper clad area of A=600 mm² and a device distance D=17 mm at 1.5 W total dissipation in the package.

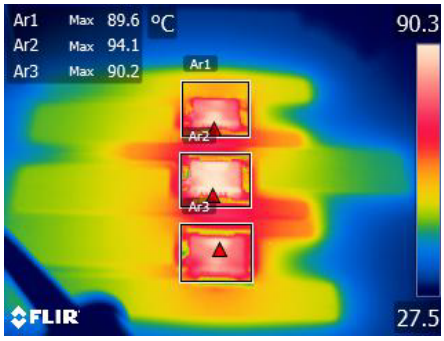
Both triangular configurations result in a more equal temperature distribution of the three BridgeSwitch devices compared to the linear configuration. For Triangular B, the temperature difference between all three devices is only 2.2 °C. This compares to 4.5 °C temperature difference between all devices in the linear configuration with the center device operating at the highest temperature.



a) Triangular A Configuration, D=17 mm, A=600 mm²



b) Triangular B Configuration, D=17 mm, A=600 mm²



c) Linear Configuration, D=17 mm, A=600 mm²

Figure 5. *Thermal Device Scans Triangular vs. Linear Configuration at 1.5 W Package Dissipation.*

External Device Supply

BridgeSwitch ICs offer self-supplied operation. This allows using a simplified auxiliary power supply with only one output rail to power the system micro-controller. However, in some circumstances it may be beneficial to supply the device externally. For example, when a given specification requires a very low no-load input power or to increase the power throughput by eliminating the power dissipation associated with internal self-supply.

Figure 6 depicts the recommended circuit for supplying the device externally. Both, the BPL and the BPH supply pins have internal shunt regulators, which clamp the BPL pin to $V_{BPL(SHUNT)}$ and the BPH pin to $V_{BPH(SHUNT)}$ when an external supply V_{SUP} provides sufficient supply current.

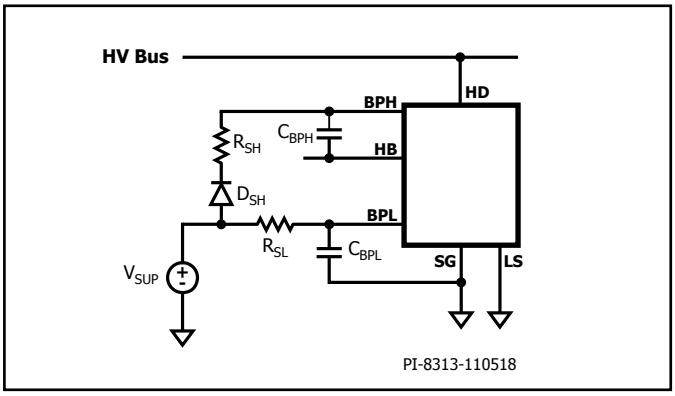


Figure 6. *External BPL Pin and BPH Pin Power Supply Example.*

Resistors R_{SH} and R_{SL} limit the external supply current to less than 12 mA (I_{SUP} = 1.5 to 2 mA recommended). External supply voltage V_{SUP} is greater than the voltage drop $V_{F(DSH)}$ of bootstrap diode D_{SH} plus the maximum shunt regulator voltage. With above considerations, the external supply parameters are:

$$V_{SUP} > V_{F(DSH)} + V_{BPSHUNT(MAX)} = 0.65\,V + 16.1\,V = 16.75\,V\,(for\ example\ 17\,V) \quad (1)$$

$$R_{SL} < \frac{V_{SUP} - V_{BPL(SHUNT)MAX}}{I_{SUP}} = \frac{17\,V - 16.1\,V}{1.5\,mA} = 600\,\Omega\,(for\ example\ 560\,\Omega) \quad (2)$$

$$R_{SH} < \frac{V_{SUP} - V_{F(DSH)} - V_{BPH(SHUNT)MAX}}{I_{SUP}} = \frac{17\,V - 0.65\,V - 16.1\,V}{1.5\,mA} = 166\,\Omega\,(for\ example\ 150\,\Omega) \quad (3)$$

It is also possible to supply only the low-side BPL pin externally. This allows saving of D_{SH} and R_{SH} with the trade-off of reducing dissipation inside the package by only approximately half due to self-supply of the high-side driver (BPH pin).

Figure 7 illustrates the benefit of supplying BridgeSwitch ICs externally with the 3-phase 300 W design platform DER-653. Allowing for device package temperature of 100 °C with an ambient temperature of 60 °C, the externally supplied inverter delivers 0.85 A_{RMS} output current. This compares to only 0.75 A_{RMS} for the same temperature rise when operating self-supplied.

External supply also reduces no-load input power of the inverter. Table 2 lists typical 3-phase inverter DC bus no-load input power levels with either self-supplied or externally supplied operation. Actual no-load input power levels for a given design depend on external circuitry such as DC bus monitoring impedance or the efficiency of the auxiliary power supply.

DC Bus Voltage	Externally Supplied	Self-Supplied
325 VDC	30 to 50 mW	330 to 370 mW

Table 2. *Inverter DC Bus No-Load Input Power using Self-Supply or External Supply.*

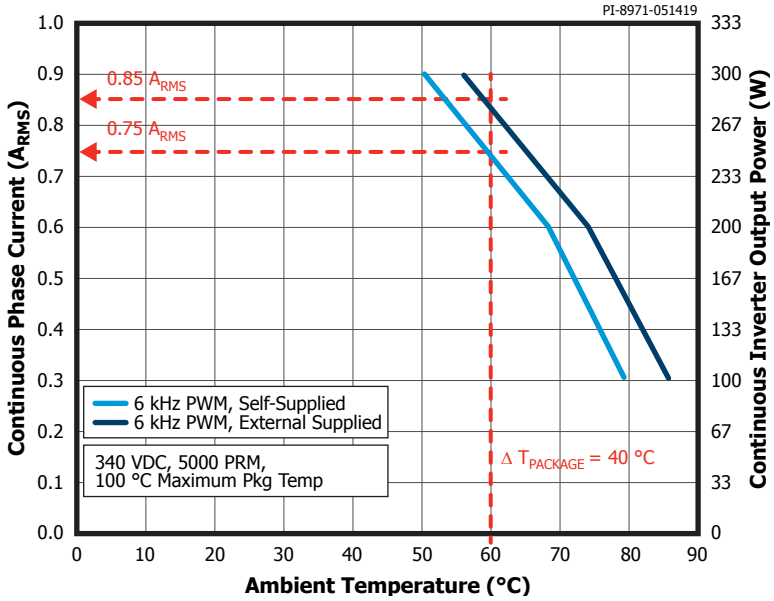


Figure 7. *Inverter Output Current with DER-653 using Self-Supply or External Supply.*

Composite DC Bus Monitoring

BridgeSwitch ICs offer DC bus overvoltage (OV) protection through its SM pin. For a typical implementation, one of the three devices in a 3-phase inverter monitors the DC bus through a resistor connected between its SM pin and the DC bus (see device HB 2 in Figure 8). Once the device detects a DC bus overvoltage fault, it inhibits switching of both integrated FREDFETs and reports the status update to the system micro-controller through the single-wire FAULT interface. The micro-controller then shuts down the entire inverter to protect the other two devices. Regular operation could resume once the device monitoring the DC bus reports clearing of the DC bus OV fault. This implementation allows using the SM pin of the other two devices for monitoring additional system parameter. For example, motor temperature or vibration.

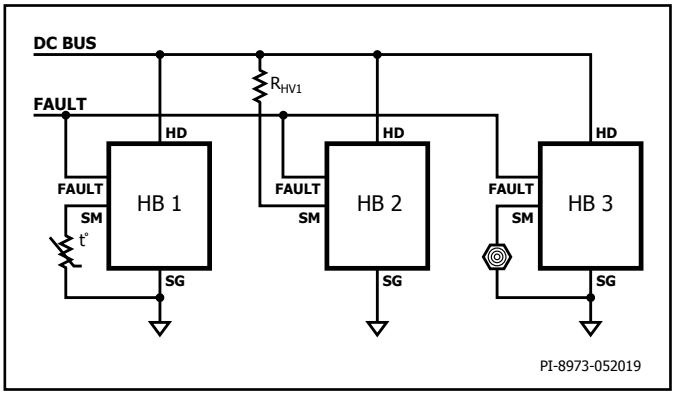


Figure 8. *DC Bus Monitoring Implementation with a Single BridgeSwitch Device.*

Motor drives that require DC bus overvoltage protection, but do not have FAULT interface communication implemented, can use composite DC bus monitoring as shown Figure 9.

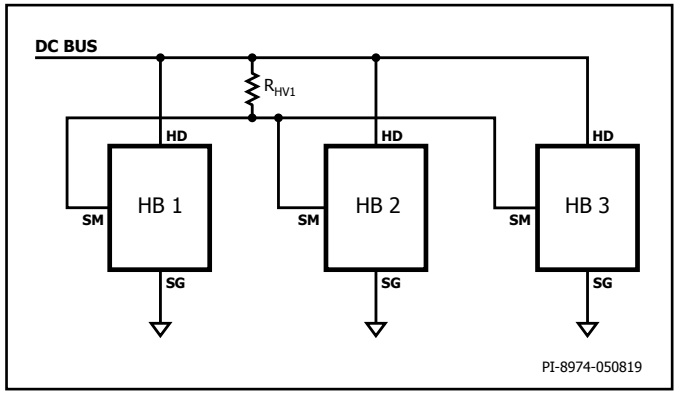


Figure 9. *Composite DC Bus Monitoring Implementation.*

Interconnected SM pins of all three devices monitor the DC bus through resistance R_{HV1}. Since the SM pin is a current based sense input, the actual DC bus over-voltage threshold V_{OV} is determined as follows:

$$V_{OV} = R_{HV1} \times 3\, I_{OV} + V_{SM} \quad (4)$$

All devices will inhibit switching as soon as the DC bus exceeds V_{OV} for at least $t_{D(OV)}$ (refer to BridgeSwitch data sheet for details). Once the DC bus voltage has reduced again and all low-side and high-side BP pins voltages are at nominal levels, the devices will enable switching again.

The specified tolerance of the High-Voltage Bus OV Threshold Current I_{OV} is ±5%. Depending on the slew rate of a given surge causing a DC bus overvoltage fault, the three devices in an inverter may consequently not inhibit switching at the same instant.

Hardware Based Motor Inrush Current Limiting (Soft-Start)

Inverters driving brushless DC motors have to cope with large motor winding inrush currents at start-up when there is no back EMF voltage. Only the motor winding impedance and the on-resistances of the power switches in the inverter limit the peak current. Therefore, either the drive inverter has to handle the high start-up currents or the system micro-controller applies a software-based soft-start function.

The low and high-side cycle-by-cycle current limit of BridgeSwitch ICs allow implementing hardware based inrush current limit function to reduce stress at start-up. The only requirement is that at least one of the two switches in the half-bridge leg operates with a continuous PWM drive signal during start-up. To implement the soft-start function, the power switch driven by a continuous PWM signal uses a cycle-by-cycle current limit threshold lower than the other switch in the half-bridge, for example 90%. Programming resistors connected to the XL pin and the XH pin allow setting the respective current limit thresholds independently (refer to Figure 12 in the BridgeSwitch family data sheet for details).

Figure 10 and Figure 11 compares motor start-up performance of the 300 W reference design DER-654 with and without soft-start. The micro-controller uses trapezoidal control with low-side block commutation and high-side PWM commutation. For this example, the inverter operates from a 310 VDC bus with an output load set to a steady-state 1.0 A_{RMS} and a motor speed of 4200 RPM.

For the case without soft-start (see Figure 10), the current limit threshold is set to 3.0 A for both power switches in all BridgeSwitch devices. At power-up, phase U motor winding current reaches the current limit threshold after approximately 9 ms and the BridgeSwitch IC terminates the low-side power switch on-cycle. Meanwhile the system micro-controller maintains the INL control signal at the high state. The low-side switch never turns on again and remains off. Consequently phase U back EMF voltage $V_{BEMF(U)}$ (proportional to motor speed) and motor current $I_{MOTOR(Phase\ U)}$ drop to 0. The motor stalls and start-up failed. For the example with soft-start implemented (see Figure 11), the current limit threshold is set to 3.0 A for all low-side switches and to 2.7 A for all high-side switches. Motor currents do not reach the low-side current limit threshold and the back EMF voltage continues to build as the motor speed increases. The motor starts up successfully and reaches steady-state speed after approximately 4.5 ms.

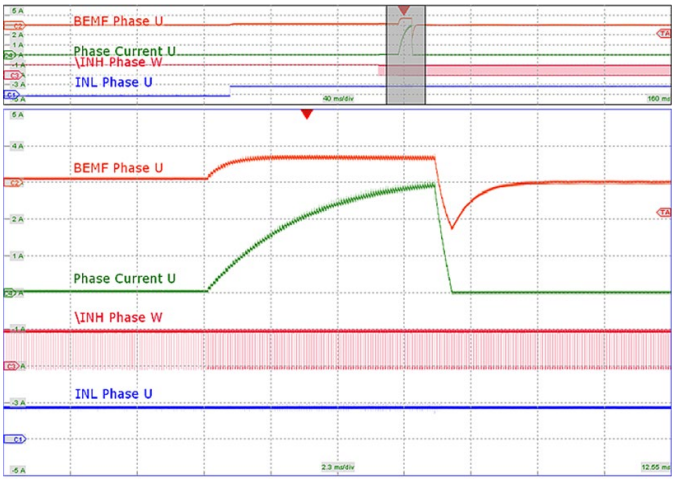


Figure 10. *Motor Start-Up without Soft-Start.*
First: $V_{BEMF(PHASE\ U)}$, 50 V / div.
Second: $I_{MOTOR(PHASE\ U)}$, 1 A / div.
Third: $V_{/INH(PHASE\ W)}$, 5 V / div.
Fourth: $V_{INL(PHASE\ U)}$, 5 V / div.
Time Scale: 2.3 ms / div. (zoom)

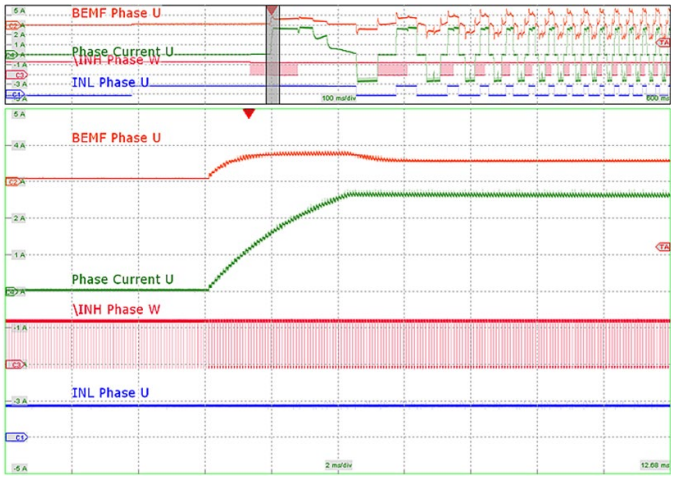


Figure 11. *Motor Start-Up with Soft-Start.*
First: $V_{BEMF(PHASE\ U)}$, 50 V / div.
Second: $I_{MOTOR(PHASE\ U)}$, 1 A / div.
Third: $V_{/INH(PHASE\ W)}$, 5 V / div.
Fourth: $V_{INL(PHASE\ U)}$, 5 V / div.
Time Scale: 2 ms / div. (zoom)

Figure 12 depicts high-side current limit operation during motor start-up with soft-start implemented. The BridgeSwitch IC terminates the high-side FREDFET on-cycle as soon as the current reaches 2.7 A. However, due to the continuous PWM signal, the high-side switch turns on again with the next falling edge on /INH and the motor current continues to flow. The motor winding current is effectively limited to 2.7 A and is well below the low-side switch current limit of 3.0 A.

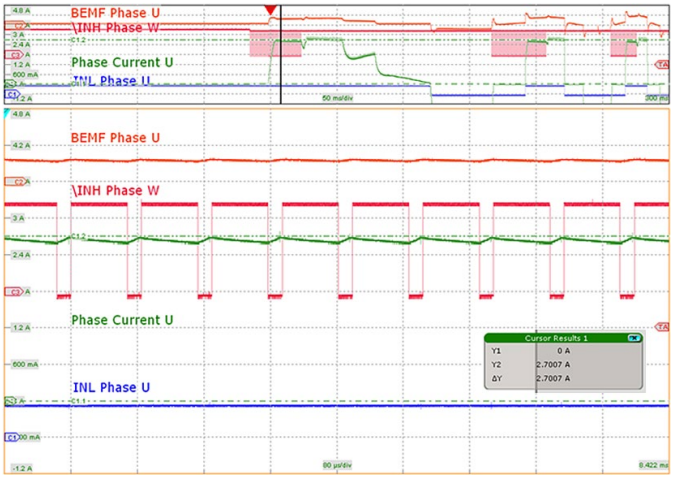


Figure 12. *High-Side Current Limit Operation at Start-Up with Soft-Start.*
First: $V_{BEMF(PHASE\ U)}$, 50 V / div.
Second: $I_{MOTOR\ (PHASE\ U)}$, 1 A / div.
Third: $V_{/INH(PHASE\ W)}$, 2 V / div.
Fourth: $V_{INL(PHASE\ U)}$, 5 V / div.
Time Scale: 80 µs / div. (zoom)

Figure 13 shows the virtual ground circuit used to measure phase back EMF voltage $V_{BEMF(U)}$ depicted in Figure 11, Figure 12, and Figure 13 with R_U=R_V=R_W=200 kΩ.

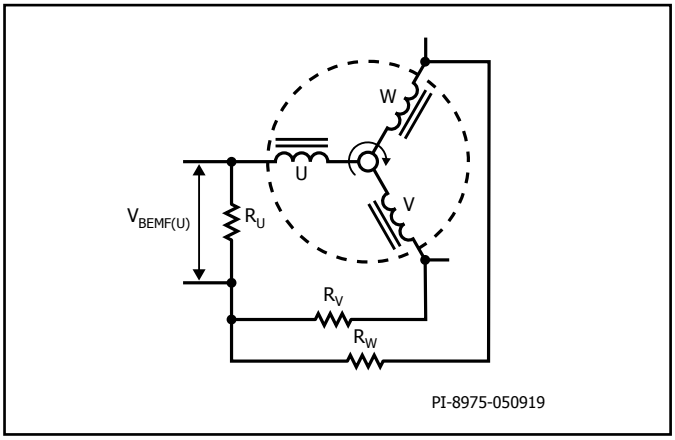


Figure 13. *Back EMF Voltage Sensing using a Virtual Ground.*

Complementary PWM Signal Operation

Certain motor control algorithms, such as sinusoidal control, may use complementary PWM signals to drive low-side and high-side switches in an inverter half-bridge leg. Benefits of such a drive scheme are a simplified PCB layout and a reduced pin count at the micro-controller.

BridgeSwitch ICs are well suited for this type of control because of the reverse polarity of the two control inputs. Low-side control input INL is active high and high-side control input /INH is active low. This allows tying both control inputs together and driving them with a single complementary PWM signal. The device internal Gate drive logic applies adaptive dead times, which prevent FREDFET cross conduction (refer to Figure 12 in the BridgeSwitch data sheet for more details). The INL input has an internal pull-down circuit and the /INH input has an internal pull-up circuit. Both prevent accidental power switch turn-on when the micro-controller does not provide a PWM signal. Connecting both inputs together may neutralize both functions. Adding an external pull-down resistor R_{PD} in complementary PWM drive mode as depicted in Figure 14 prevents possible accidental, noise induced FREDFET switching. The recommended value is 10 kΩ to 100 kΩ.

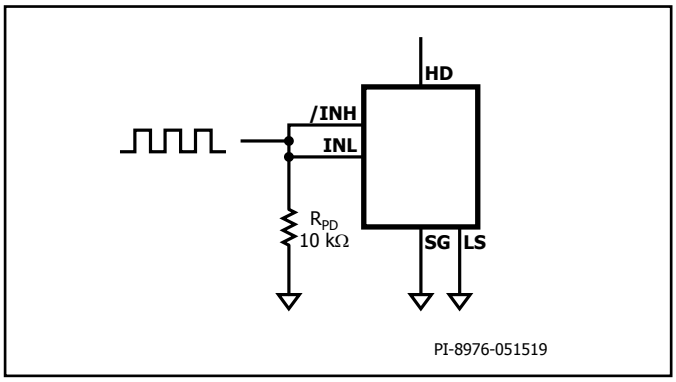


Figure 14. *Complementary PWM Signal Drive.*

The following example waveform plots illustrate complementary PWM mode operation with the AC fan reference design DER-749 operating from a 310 VDC bus and 0.15 A_{RMS} inverter load current. DER-749 employs the 3-phase sinusoidal BLDC motor controller PT2505 with a PWM frequency of 20 kHz. Its respective phase high-side PWM output drives the combined INL and /INH logic input of BridgeSwitch. Pull-down resistor R_{PD}=10 kΩ.

Figure 15 depicts device power-up with complementary PWM mode operation. An internal high-voltage current source connected to the HD pin charges the BPL pin capacitor to its nominal value as soon as the input voltage becomes available. A second high-voltage current source responsible for supplying the HS driver starts charging the BPH pin capacitor as soon as the controller applies the complementary PWM signal to the INL and /INH inputs. This turns on the low-side FREDFET allowing the capacitor charge current to flow. Once the BPH pin voltage reaches its nominal value, the device enables high-side FREDFET switching and motor phase current starts to flow.

Figure 16 illustrates a motor drive start-up with PWM signals and phase motor winding currents shown for phases U and V.

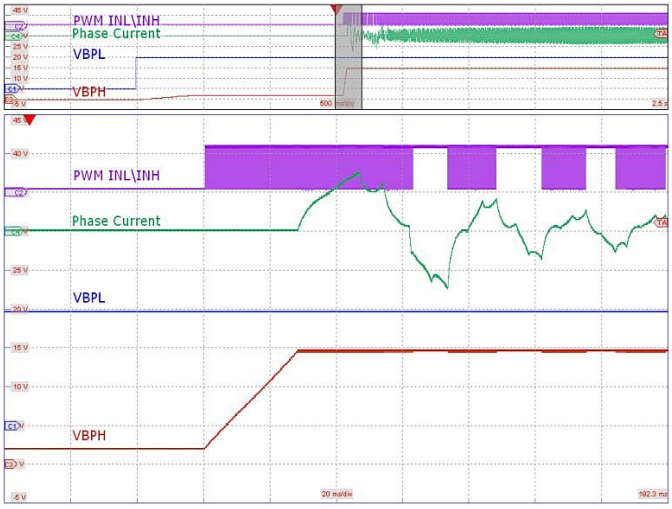


Figure 15. *Complementary PWM Mode Device Power-Up.*
First: $V_{PWM(INL\INH)}$, 5 V / div.
Second: $I_{MOTOR(PHASE\ U)}$, 400 mA / div.
Third: $V_{BPL(PHASE\ U)}$, 5 V / div.
Fourth: $V_{BPH\ (PHASE\ U)}$, 5 V / div.
Time Scale: 20 ms / div. (zoom)

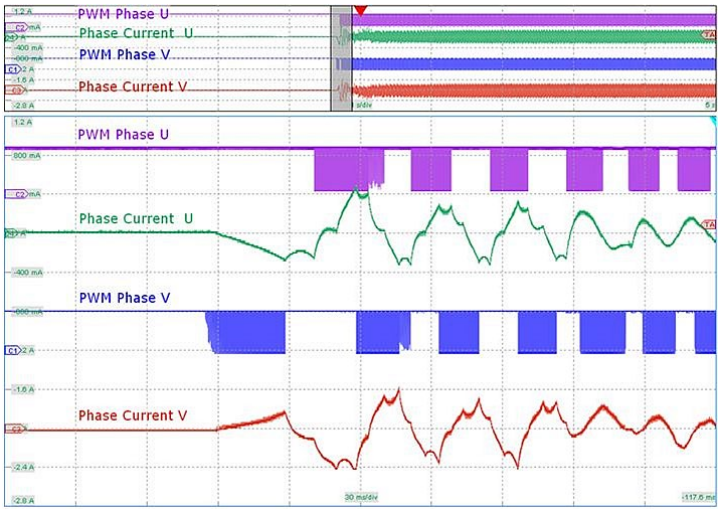


Figure 16. *Complementary PWM Mode Motor Start-Up.*
First: $V_{PWM(PHASE\ U)}$, 5 V / div.
Second: $I_{MOTOR(PHASE\ U)}$, 400 mA / div.
Third: $V_{PWM(PHASE\ V)}$, 5 V / div.
Fourth: $I_{MOTOR(PHASE\ V)}$, 400 mA / div.
Time Scale: 30 ms / div. (zoom)

Figure 17 depicts complementary PWM signal, motor winding current and half-bridge voltage in steady-state operation for one of the three phases. Figure 18 illustrates motor stopping with PWM signals and phase motor winding currents shown for phases U and V. The PT2505 controller high-side PWM output sets the complementary PWM signal to active high with its motor speed control input VSP set to 0. This effectively disconnects the motor from the DC bus by turning off all high-side FREDFETs. The low-side FREDFETs remain on and phase currents fall to 0 causing the motor to stop rotating.

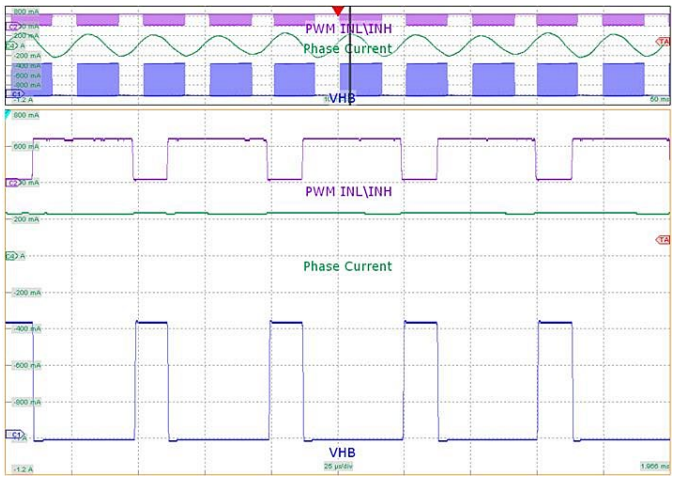


Figure 17. *Complementary PWM Mode Steady-State Operation.*
First: $V_{PWM(INL\INH)}$, 5 V / div.
Second: $I_{MOTOR(PHASE\ U)}$, 200 mA / div.
Third: $V_{HB(PHASE\ U)}$, 100 V / div.
Time Scale: 25 µs / div. (zoom)

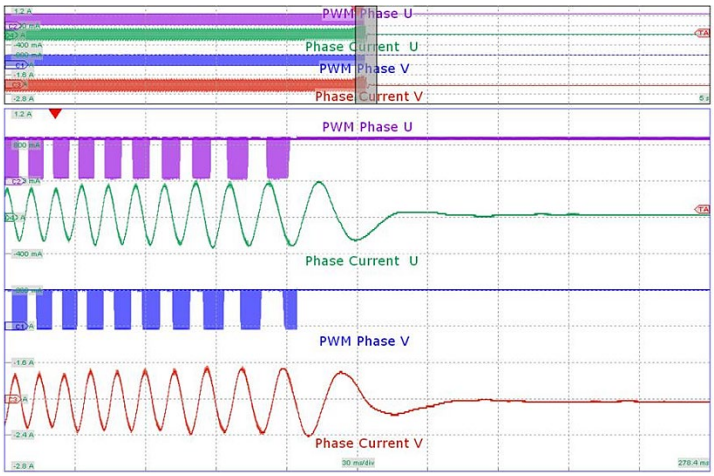


Figure 18. *Complementary PWM Mode Motor Stopping.*
First: $V_{PWM\ (PHASE\ U)}$, 5 V / div.
Second: $I_{MOTOR\ (PHASE\ U)}$, 400 mA / div.
Third: $V_{PWM\ (PHASE\ V)}$, 5 V / div.
Fourth: $I_{MOTOR\ (PHASE\ V)}$, 400 mA / div.
Time Scale: 30 ms / div. (zoom)

PWM Signal Polarity Inverter for High-Side /INH Input

BridgeSwitch ICs feature PWM control inputs with reverse polarity for controlling the switch state of the low-side and the high-side FREDFET. This enables optional complementary PWM mode operation. For applications that drive FREDFETs independently, a simple software modification in the micro-controller changes the PWM signal polarity. Applications that use hardware based motor control ICs, which do not allow changing PWM signal polarity, can use a simple polarity inverter as depicted in Figure 19.

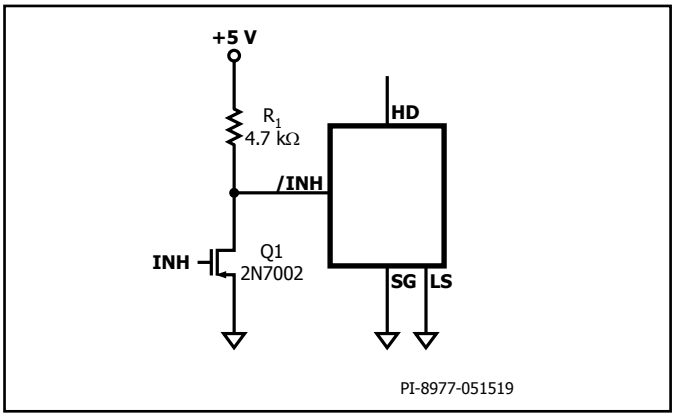


Figure 19. *PWM Signal Polarity Inverter for /INH Input.*

Inverter Inhibit Function

Some motor drive applications may require an inhibit function to prevent the inverter from starting or to stop operation immediately. For example, during a micro-controller self-check of PWM signal outputs or for implementing passive breaking without the interaction of the micro-controller. Figure 20 depicts a simple implementation of this function with BridgeSwitch. It makes use of the integrated XL pin short circuit protection (refer to the BridgeSwitch data sheet for more details). Resistors R_{XL1}, R_{XL2}, and R_{XL3} set the desired low-side cycle-by-cycle current limit threshold. Applying the inhibit signal turns on transistor Q1 and short-circuits the XL pins to ground. BridgeSwitch detects the excess currents flowing out of the XL pins and disables FREDFET switching for as long as the inhibit signal is present. Diodes D1, D2, and D3 prevent low-side current limit threshold interactions due to slight part-to-part variations of respective XL pin voltage levels. Figure 21 and Figure 22 illustrate an exemplary use of the inhibit function with reference design DER-654 operating at 310 VDC bus and a steady-state output load current of 0.5 A_{RMS}. All devices stop switching and phase currents drop to zero instantaneously with the inhibit signal applied as depicted in Figure 21 (showing phase U and V currents for representation). FREDFET switching commences as soon as the inhibit signal disappears and the motor starts up again as depicted in Figure 22.

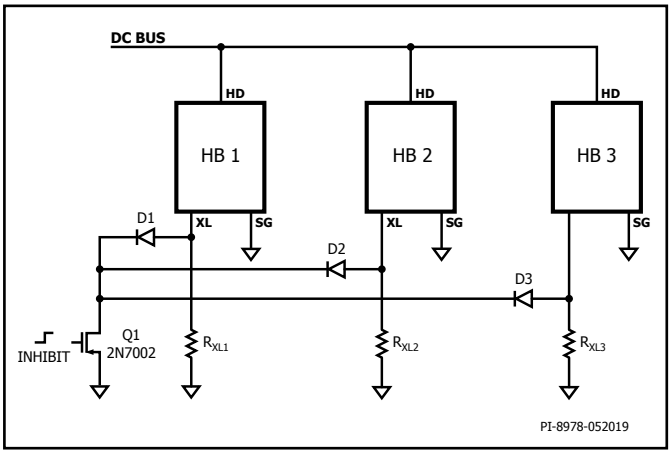


Figure 20. *Inhibit Function for 3-Phase BridgeSwitch Inverter.*

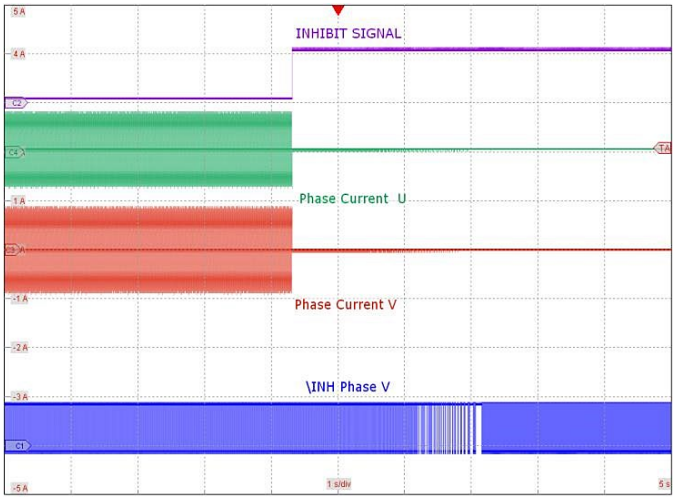


Figure 21. *Inhibit Signal Active.*
First: $V_{INHIBIT}$, 5 V / div.
Second: $I_{MOTOR(PHASE\ U)}$, 1 A / div.
Third: $I_{MOTOR(PHASE\ V)}$, 1 A / div.
Fourth: $V_{\backslash INH\ (PHASE\ V)}$, 5 V / div.
Time Scale: 1 s / div.

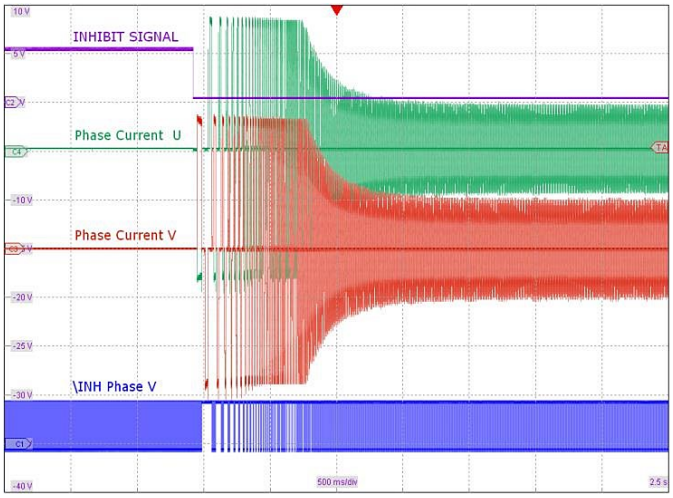


Figure 22. *Inhibit Signal Removal.*
First: $V_{INHIBIT}$, 5 V / div.
Second: $I_{MOTOR(PHASE\ U)}$, 1 A / div.
Third: $I_{MOTOR(PHASE\ V)}$, 1 A / div.
Fourth: $V_{\backslash INH\ (PHASE\ V)}$, 5 V / div.
Time Scale: 500 ms / div.

Determining Operating Junction and PCB Temperature

The integrated two-level FREDFET temperature reporting of BridgeSwitch devices allows determining the junction temperature at a given load and ambient temperature condition with the following method. It makes use of the LS FREDFET Junction Temperature Warning reported through the FAULT interface ("XXX 01 XX" status update, see Table 3 or BridgeSwitch data sheet for details) when the junction temperature reaches T_{WA} = 125 °C.

1. Load inverter with target continuous load current I_{RMS} and let it settle at the target ambient temperature T_{AMB}.
2. Slowly raise ambient temperature until the FAULT output reports "LS FREDFET Temperature Warning" and note ambient temperature $T_{AMB(WARNING)}$ at which the device reports the warning. The device junction temperature is T_{WA} at this point.
3. Derived junction temperature T_J at target load current I_{RMS} and ambient temperature T_{AMB} is:
   $T_J = T_{AMB} + T_{WA} - T_{AMB(WARNING)}$ (5)

Figure 23 illustrates the application of this method with reference design DER-653. It depicts the temperature of several points of interest (ambient, PCB, and device package) measured with thermocouples over time. For this measurement, the inverter resides inside a thermal chamber and delivers an output load current of 0.9 A_{RMS}.

Once the device temperature settled at the target ambient temperature T_{AMB} = 36 °C, the thermal chamber slowly increases ambient temperature until the device reports a Junction Temperature Warning. For this example, the reporting occurs at $T_{AMB(WARNING)}$ = 54 °C. The top of the device package temperature is at $T_{PKG(WARNING)}$ = 114 °C at this point. The operating junction T_J temperature of reference design DER-653 at 0.9 A_{RMS} load current and 36 °C ambient temperature is therefore with (5): T_J = 36 °C + 125 °C - 54 °C = 107 °C.

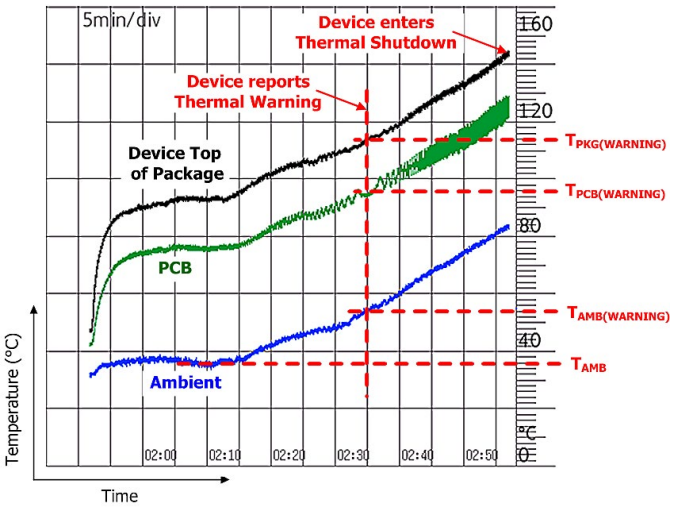


Figure 23. *System Temperature Measurements with BridgeSwitch.*

The exposed pads of the device package, which facilitate heat transfer from the FREDFET switches, have an excellent thermal coupling to the PCB. This allows monitoring the PCB temperature through the device instead of using a thermal sensor such as an NTC. The measurement results depicted in Figure 23 show that the device temperature correlates well with the PCB temperature. For the above example, the PCB temperature is at $T_{PCB(WARNING)}$ = 96 °C when the BridgeSwitch IC reports the Junction Temperature Warning through the FAULT interface. Adjusting the size of the PCB copper clad area connected to the exposed pads allows fine-tuning the relationship between device and PCB temperature. The system micro-controller can use this information and take action in applications where the PCB temperature may not exceed a certain level for safety reasons.

Troubleshooting Guide

The Fault interface can provide valuable hints during debugging of an inverter using BridgeSwitch. When connected to a 3.3 V or 5 V supply through for example a 10 kΩ resistor, it is possible to monitor the FAULT pins with an oscilloscope probe and receive information on what might preventing the inverter from operating as expected. Table 3 summarizes how all detected status updates (including device level faults) are encoded and reported.

Status	Parameter	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6
High-voltage bus OV	I_{OV}	0	0	1	X	X	X	X
High-voltage bus UV 100%	I_{UV100}	0	1	0	X	X	X	X
High-voltage bus UV 85%	I_{UV85}	0	1	1	X	X	X	X
High-voltage bus UV 70%	I_{UV70}	1	0	0	X	X	X	X
High-voltage bus UV 55%	I_{UV55}	1	0	1	X	X	X	X
System thermal fault	$V_{TH(TM)}$	1	1	0	X	X	X	X
LS Driver not ready[1]	n/a	1	1	1	X	X	X	X
LS FET thermal warning	T_{WA}	X	X	X	0	1	X	X
LS FET thermal shutdown	T_{SD}	X	X	X	1	0	X	X
HS Driver not ready[2]	I_{COM}	X	X	X	1	1	X	X
LS FET over-current	$V_{X(TH)}$	X	X	X	X	X	1	X
HS FET over-current	$V_{X(TH)}$	X	X	X	X	X	X	1
Device Ready (no faults)	n/a	0	0	0	0	0	0	0

Table 3. *Status Word Encoding.*

NOTES:
1. Includes XL pin open/short-circuit fault and IPH pin to XL pin short-circuit.
2. Includes internal communication loss, supply out of ranage, and XH pin open/short circuit fault.

Table 4 lists common symptoms for inverter misbehavior, their possible causes, and how to address them.

Symptom	Possible Cause	What to Do
Inverter does not start up.	Device supply voltage is not at nominal level when MCU applies MCU signals. Effective capacitance of BYPASS capacitors is too low at 15 V. BYPASS capacitors do not meet minimum capacitance requirements.	• Verify BYPASS voltages V_{BPL} and V_{BPH} are at nominal levels. • Check DC bias characteristic rating of BPL and BPH pin capacitors at 15 V. • Verify start-up sequence follows recommended device power-up sequence (refer to Figure 9 in the data sheet). • Verify BYPASS capacitors meet minimum capacitance requirements (refer to Figures 7 and 8 in the data sheet).
Device temperature is too high.	Device placement is not optimal. PCB copper clad area is too small. Chosen device is too small for given phase RMS current or ambient temperature requirements.	• Consider optimized device placement (for example triangular configuration). • Consider using a lower PWM frequency. • Supply BYPASS pins externally (refer to Figure 5). • Increase copper area used for heat sinking. • Add thermal vias between solder and component side copper clads. • Verify that soldering of exposed pads to PCB is correct. • Use thicker copper (for example 70 μm). • Use a larger device size.
Motor stalls at start up.	Device current limit level is too low. Soft-start is missing.	• Increase cycle-by-cycle current limit thresholds through XL and XH pin resistors. • Implement hardware-based soft-start. • Choose a larger device size.
Inverter no-load input power is too high.	Devices use internal self-supply.	• Use external power supply (refer to Figure 6).
FAULT interface continuously reports "HS Driver Not Ready"	BYPASS voltage V_{BPH} is too low. LS FREDFET on time is too short. XH pin resistor is placed too far from device. XH pin is open circuit or shorted to HB.	• Verify V_{BPH_HB} voltage is at the nominal level (typ. 14.5 V relative to HB). • Verify LS FREDFET control input INL is high for at least $t_{INLH(COM)}$ (refer to Figure 24 in the data sheet). • Minimize PCB loop between XH pin, XH selection resistor, and HB pins.
HB pin voltage with respect to LS pin is dropping below absolute maximum rating.	Large parasitic inductances in the PCB layout cause voltage spikes at HS FREDFET turn-off. Placement of measurement probe picks up noise.	• Add a local DC bus decoupling capacitor between DC bus positive and negative planes close to the device. • Verify measured negative voltage spike is real.
Erroneous switching when using composite PWM signal driving INL and /INH pins shorted together.	Excessive noise present on the PWM signal provided by the MCU causes false FREDFET turn-on.	• Reduce PCB loop between MCU PWM output and combined INL and /INH pins. • Add pull-down resistor to the interconnected INL and /INH inputs (see Figure 14).
Motor spins in a direction opposite to what is expected.	One or two motor phases may have improper connection to the inverter. One phase may temporarily stop switching.	• Verify motor phase connections. • Verify DC bus monitoring impedance uses correct value.

Table 4. *Troubleshooting Guide.*

Revision	Notes	Date
A	Initial release.	05/19

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