Application Note AN-87
BridgeSwitch Family

1-Phase BLDC Motor Drive

Introduction

The BridgeSwitch™ family of integrated half-bridges dramatically simplifies the development and production of high-voltage inverters for permanent magnet (PM) or brushless DC (BLDC) motor drives. The half-bridge architecture enables BridgeSwitch design flexibility for driving single or multi-phase motors. The high-level of integration, highest performance without heat sink, and integrated safety and reliability make it ideally suitable for the latest generation of high performance inverters.

BridgeSwitch incorporates two high-voltage N-channel 600 V rated power FREDFETs with low and high-side drivers in a single small-outline package. The internal power FREDFETs offer ultrasoft and ultrafast diodes ideally suited for hard switched inverter drives. Both drivers are self-supplied eliminating the need for an external auxiliary power supply. A unique feature provides an instantaneous phase current output signal simplifying implementation of sensor-less control schemes. The low-profile, compact footprint surface mount package offers extended creepage distances and allows heat sinking of both power FREDFETs through the printed circuit board.

BridgeSwitch offers internal fault protection functions and external system level monitoring. Internal fault protection includes cycle-by-cycle current limit for both FREDFETs and two level thermal overload protection. External system level monitoring includes DC bus sensing with four under-voltage levels and one over-voltage level as well as driving external sensors such as an NTC. The bi-directional bussed single wire status interface reports observed status changes.

BridgeSwitch is very well suited for 1-phase motor drive applications. The high level of integration and simplicity of design enables a significant reduction in the overall component count resulting in low system cost and a highly compact design.

Scope

The application note describes the motor control theory and inverter drive implementation for a 1-phase (BLDC) motor drive using BridgeSwitch. The presented theory and implementation covers specifically the conventional control of a single-winding 1-phase BLDC motor using a full-bridge inverter topology.

The document contains the following sections:

- 1-Phase BLDC Motors Overview
- 1-Phase BLDC Motor Control
- Design Example
- Key Application Design Considerations

1-Phase BLDC Motors Overview

1-phase BLDC motors are cost-effective alternatives to 3-phase BLDC motors for applications that requires simplicity and low-cost while providing smaller size, better performance and higher reliability when compared to conventional AC motors. Overall system cost is reduced (versus 3-phase) due to a simple and inexpensive motor construction, fewer switching transistors, and only a single hall sensor, which allows using a simple and low-cost micro-controller. 1-phase BLDC motors are attractive for low power applications where cost considerations outweigh performance.

Figure 1. 1-Phase BLDC Motor.

1-Phase BLDC Motor Control

In principle, 1-phase BLDC motors have the same number of coils/slots as poles in a single winding pattern. Thereby, the coils are connected in series and wound on the stator in a vice-versa manner. In order to generate torque over one electrical period of the motor, the current has to alternate its polarity, and consequently, the motor windings must be fed by a full bridge inverter. Figure 2 and Figure 3 shows a conventional 1-phase BLDC machine and the full bridge inverter circuit.

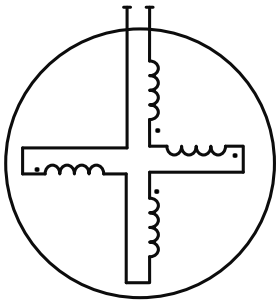


Figure 2. Single Winding 4-pole, 4-slot 1-Phase BLDC Motor Representation.

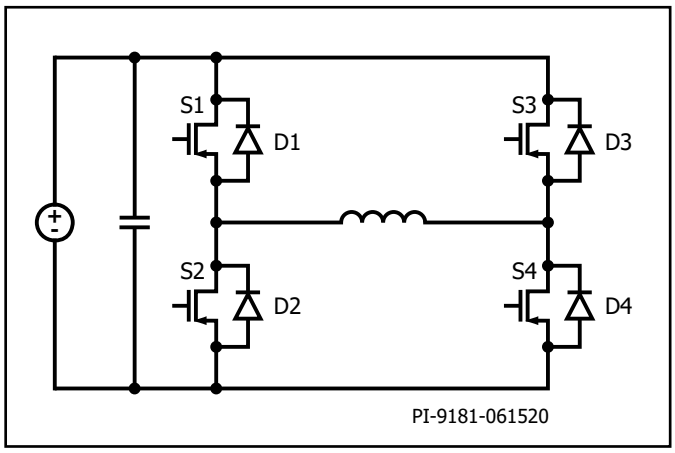


Figure 3. Full Bridge Inverter for a 1-Phase BLDC Motor.

Torque is produced as a direct consequence of power converted through the back EMF. The power converted at any instant is the product of the drive current and back EMF. The average power converted for a 1-phase BLDC motor is the average of that product over one electrical cycle, and generally depends on the shape of both the back EMF $E(t)$ and the drive current $I(t)$. The product of torque (τ) and speed (ω) of the motor represents the mechanical output power.

The following equations summarize the power conversion and torque generation based on these fundamentals.

$$P(t) = I(t) \times E(t) = \tau(t) \times \omega(t)$$

$$P_{AVG} = \frac{1}{T}\int_{O}^{T} I(t) \times E(t) \times d(t) = \tau_{AVG} \times \omega_{AVG}$$

The back EMF voltage V_{EMF} and the motor winding voltage waveform V_P applied on the full bridge inverter over one electrical period are shown in Figure 4. The polarity of the applied winding voltage matches the polarity of the back EMF to generate useful torque.

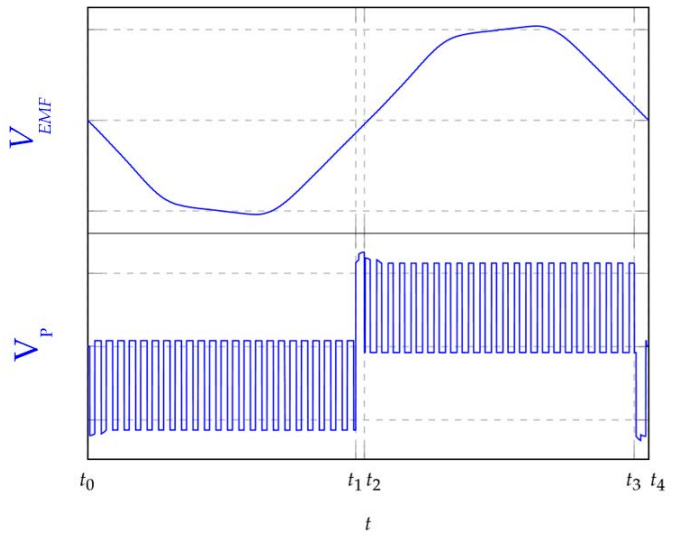


Figure 4. Electrical Signals for a 1-Phase BLDC Motor.

The commutation relies on the rotor position feedback which is indirectly represented electrically by the back EMF. In conventional 1-phase control, typically one hall sensor IC is used to detect the back EMF signal transitions. The hall sensor feedback is then fed to a controller to generate commutation signals to the inverter.

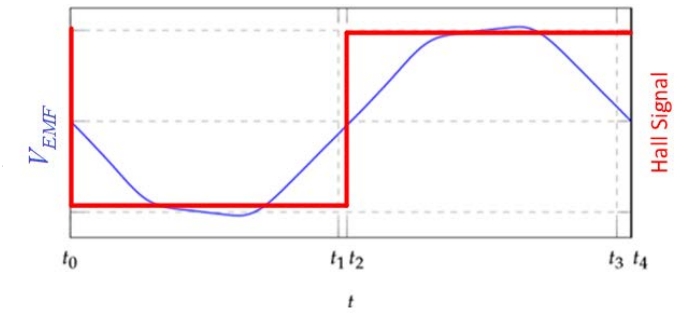


Figure 5. Hall Sensor Signal vs. Back EMF.

One conventional 1-phase BLDC motor control strategy is commonly referred to as square wave control, or block commutation. The square wave control produces a square wave shaped output voltage across the 1-phase load. This control type has a very simple control logic. Hence, it is considered the simplest control strategy. Below describes the commutation principle of a square wave PWM-based control where voltage regulation is performed by transistor switches using pulse-width modulation. The following control principle operation is analyzed under the assumption of ideal circuit conditions.

The following commutation sequence explanation refers to the full bridge inverter depicted in Figure 3 and the electrical signals over one period depicted in Figure 4. Basically, it consists of two commutation sequences over one electrical cycle: power switches S3 – S2 energizes the motor winding during negative portion of the back EMF and power switches S1 – S4 energizes the motor winding during the positive portion of the back EMF.

During the time interval ($t_0 - t_1$), the back EMF voltage is negative. To generate a positive torque, the current has to be fed to the motor through the switches S2 and S3. The low-side switch (S2) is turned on during the whole time interval while the high-side switch (S3) assumes the role of the PWM switch. During S3 PWM-OFF times, the body diode of S4 provides the freewheeling path for the phase current.

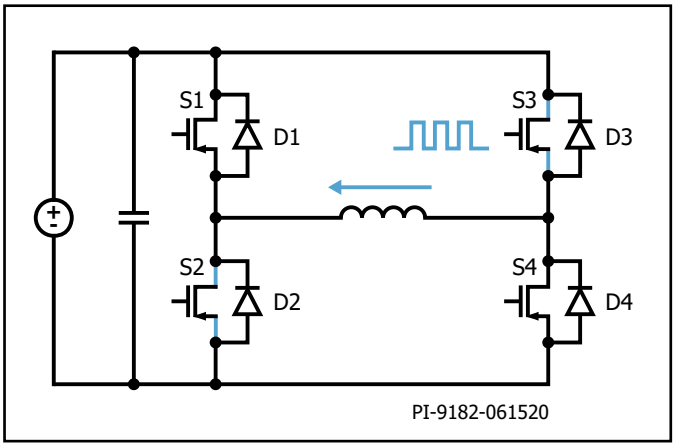


Figure 6. First Commutation Period ($t_0 - t_1$).

At t_1, switches S2 and S3 are turned off, and S1 and S4 are now responsible for the motor supply. In the time interval ($t_1 - t_2$), the phase current has to change its polarity and as long as it has negative polarity, the current will charge the DC link capacitor and produce a negative current.

During the time interval ($t_2 - t_3$), the second commutation period occurs when the back EMF is positive. To generate a positive torque, the current has to be fed to the motor through the switches S1 and S4. The low-side switch (S4) is turned on during the whole time interval while the high-side (S1) assumes the role of the PWM switch. During S1 PWM-OFF times, the body diode of S2 provides the freewheeling path for the phase current.

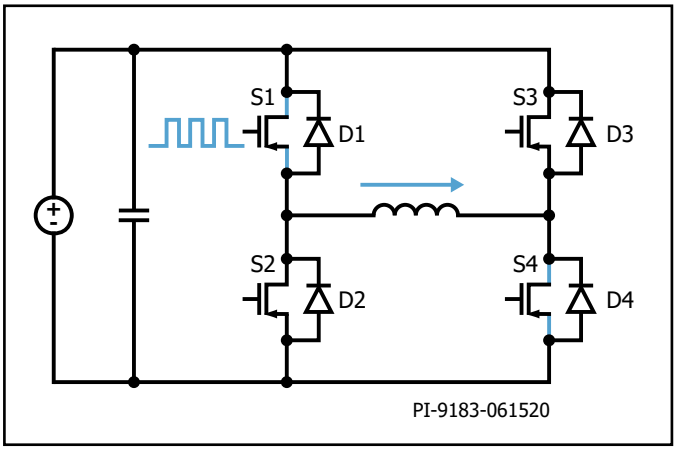


Figure 7. Second Commutation Period ($t_3 - t_4$).

Figure 8 depicts the translated commutation timing diagram of the commutation sequence described. This commutation diagram serves as the basis of the implementation of the control strategy in the software.

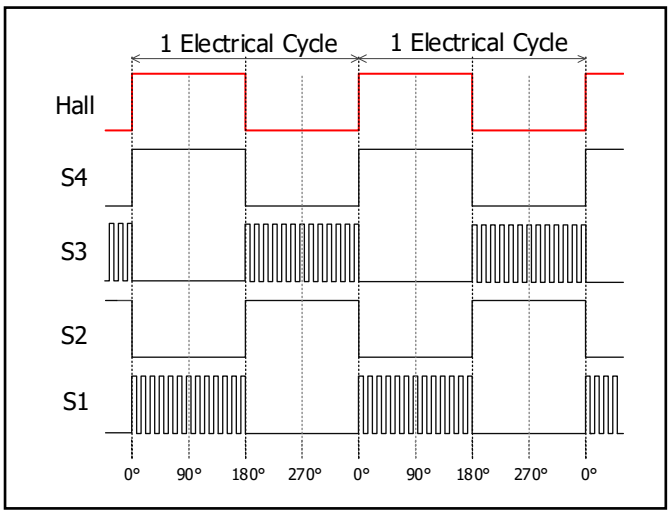


Figure 8. Conventional PWM-Based Control Commutation Timing Diagram.

It is also possible to use complementary PWM signal operation with the square-wave control strategy introduced. In that case, the corresponding high-side and low-side power switches of each half-bridge are switching in complementary fashion. The performance benefit of this type of control is improved inverter efficiency from active rectification during the motor phase current freewheeling period whenever the high-side power switch turns OFF. Figure 9 depicts the typical commutation timing.

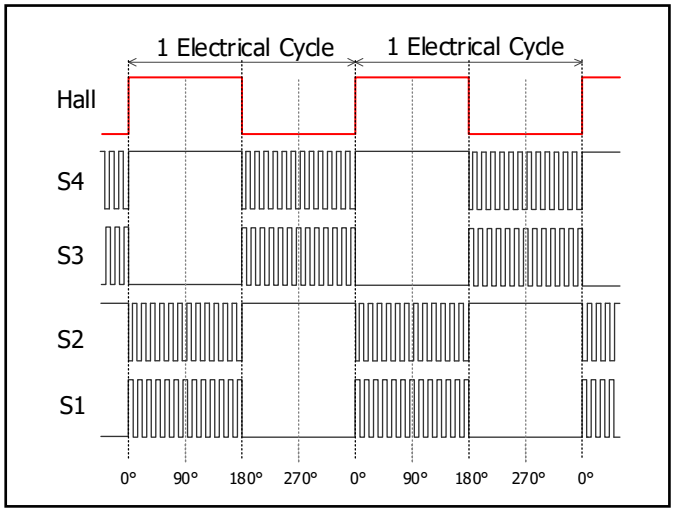


Figure 9. Complementary PWM Control Commutation Timing Diagram.

One of the key benefits of BridgeSwitch ICs is that they are well suited for complementary PWM drive. The reverse polarity of the two control inputs (Active HIGH for low-side control input, INL and Active LOW for high-side control input, /INH) allows tying both control inputs together and driving them with a single complementary PWM signal. The device internal adaptive dead time prevents FREDFET cross conduction, and the internal pull-down circuit for the INL input and internal pull-up circuit for the /INH input prevent accidental power switch turn ON, when a control signal is not provided. The benefits of such a drive implementation are reduced micro-controller pin count or I/O resources as well as simplified PCB layout.

The commutation diagram depicted in Figure 10 shows the corresponding complementary PWM commutating timing diagram with the BridgeSwitch inverter where each half-bridge device is driven using only a single PWM signal resulting in a simplified control implementation.

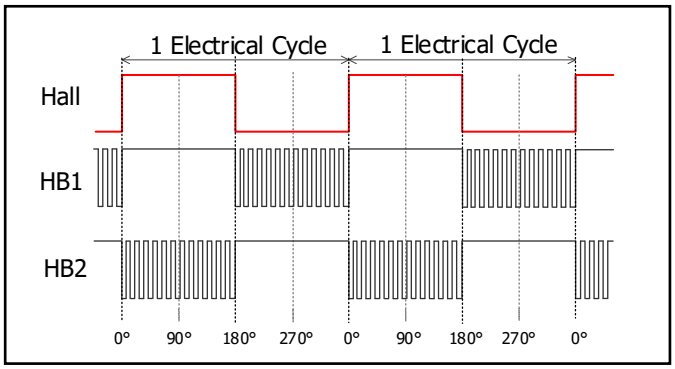


Figure 10. Complementary PWM Control Commutation Implementation with BridgeSwitch Inverter.

Application note AN-83 provides a detailed document regarding complementary PWM signal operation with BridgeSwitch. The design example report of the application example described in this document illustrates complementary PWM signal operation with a 1-phase BLDC motor. The documents are available at www.power.com: https://motor-driver.power.com/products/bridgeswitch-family/bridgeswitch/

On a different note, it is important to remember that there are two common variants of brushless permanent magnet synchronous motors. In popular literature BLDC is used to refer to a trapezoidal motor (with trapezoidal shaped back EMF); and PMSM is used to refer to a sinusoidal motor (with sinusoidal shaped back EMF). The trapezoidal and sinusoidal motors are constructed in different ways but as far as torque production and back EMF generation is concerned, the motors differ only in the shape of the rotor-stator flux linkage. This difference can be created by changing the way the winding is distributed in the stator slots and adjusting the rotor construction and magnetic design. Practically, sinusoidal motors can be difficult to make and are thus more costly, while low-cost motors tend to have more of the characteristics that lead to a trapezoidal back EMF.

In any of these two common variants, the fundamental mechanism by which torque is produced is identical regardless of the type. If a motor can be categorized as trapezoidal or sinusoidal – and ideal drive currents should be forced into it – the motor will produce "ideal" torque. Typically, motors with a trapezoidal back EMF are driven with square-wave commutation, while motors with more sinusoidal back EMF are driven with sinusoidal commutation.

Figure 11 shows the ideal back EMF waveforms of trapezoidal and sinusoidal motors normalized to an RMS value of 1.

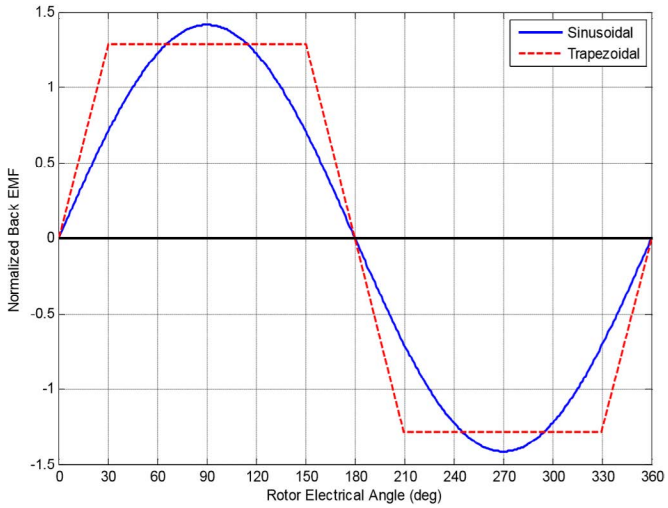


Figure 11. Ideal Sinusoidal vs. Trapezoidal Back EMF Waveforms.

While either type of motor can be driven by any arbitrary current waveform, the torque produced in each case will be different. The motor efficiency will be affected, and the power the inverter can deliver will be affected. The effects of different current drives on different motor variants are outside the scope of this document.

Generally, 1-phase motor types are trapezoidal simply because of the simple and cheap construction. Therefore, these motors target simple and low-cost applications. In practical applications, the 1-phase BLDC motor is commonly driven by either a conventional square-wave current or a trapezoidal-shaped current which resembles the actual motor back EMF shape. The latter control strategy is better, as it produces the ideal torque while reducing the overall harmonic distortion.

An example software control implementation of the common control strategies mentioned is described in the Appendix section. The BridgeSwitch inverter application example described in this document makes use of one of the software control implementations mentioned.

Design Example

The schematic shown in Figure 12 is that for a 1-phase inverter employing two fully-featured BRD1260C devices. The design is rated for a 0.22 A_{RMS}, 30 W continuous inverter output power. It is up to 95% efficient as a highly compact design in a 25 x 30 mm inverter size. The design exhibits an excellent thermal performance of less than 35 °C package temperature rise above ambient at the rated current with a DC input voltage of 310 V, running on a trapezoidal current drive at 18 kHz switching frequency.

The board incorporates a simple control interface to the external controller facilitating the inverter control inputs. Additional features include a system sensing input, instantaneous phase current output and a single wire status update communication bus. In addition, an optional input for low-side device external-bias operation is provided to reduce no-load input power.

This application example is published as a BridgeSwitch reference design: DER-873. The reference design contains the complete engineering report describing inverter specifications, circuit schematic, bill of materials, printed circuit board layout, the inverter performance, inverter manual, and the bench test setup used.

The BridgeSwitch family data sheet covers the technical details including the functional description and the circuit part selection.

The data sheet including other technical documents and the design example report can be downloaded at www.power.com: https://motor-driver.power.com/products/bridgeswitch-family/bridgeswitch/

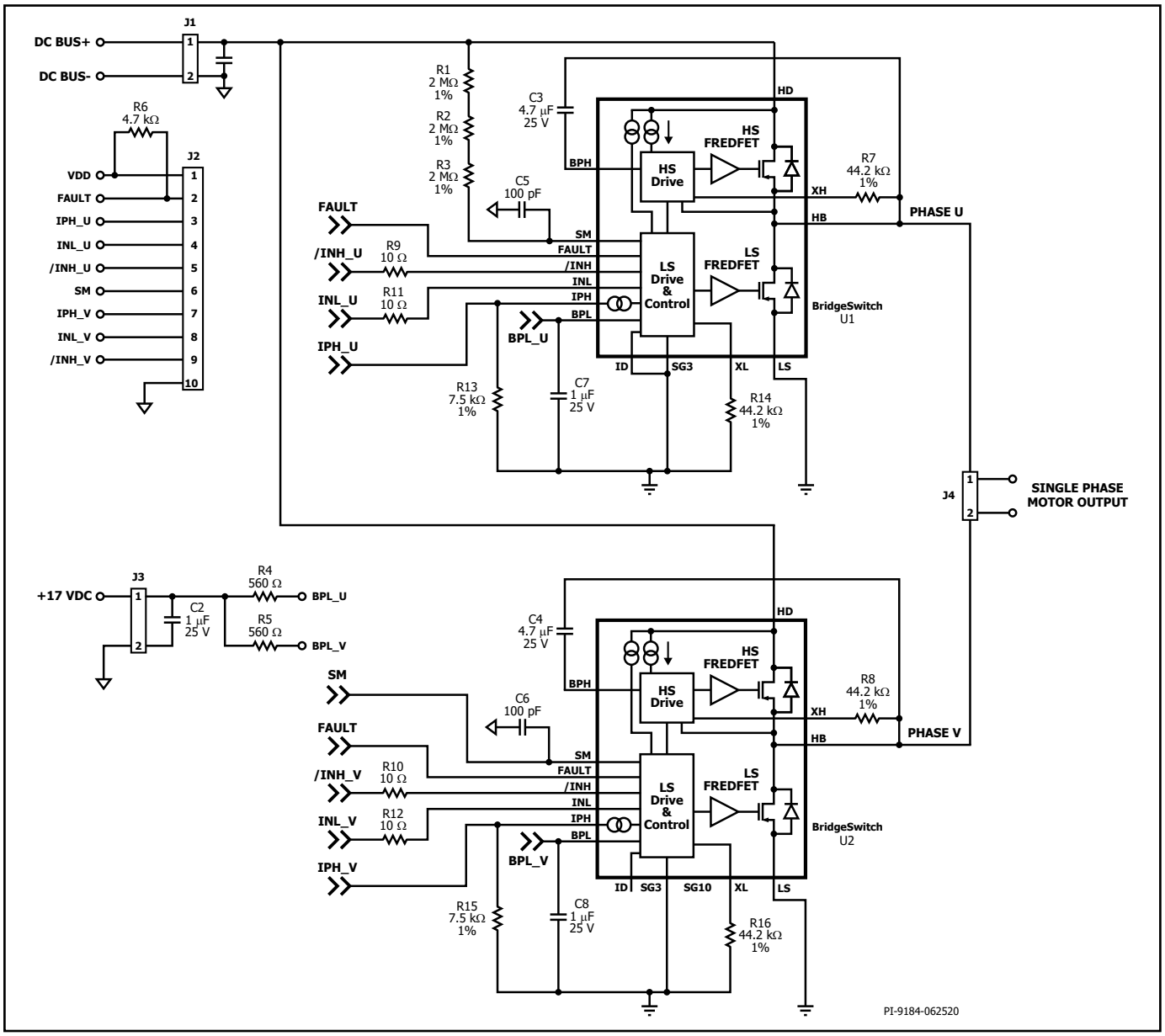


Figure 12. 1-Phase Inverter Circuit Design Example.

Circuit Description

The two BridgeSwitch devices (BRD1260C) U1 and U2 form the 1-phase inverter in a full-bridge configuration. The selected part supports the continuous motor RMS current requirement of 0.22 A_{RMS} for a 30 W inverter design. The half-bridge point of each device connects to a single winding 1-phase high-voltage BLDC motor through the connector J4.

The high-voltage DC input and power ground connect to the input connector J1. A high-voltage film capacitor C1 provides the local decoupling of the high-voltage DC link input provided externally to the inverter board.

Capacitors C7 and C8 provide self-supply decoupling for the integrated low-side driver for devices U1 and U2 respectively. The chosen capacitance follows the recommendation for BPL pin of 1 µF.

Capacitors C3 and C4 provide self-supply decoupling for the integrated high-side driver for devices U1 and U2 respectively. The chosen BPH pin capacitance is sufficient for the device to operate in self-supply up to a minimum of 1 kHz high-side PWM frequency up to 100 % duty ratio taking into account the DC bias effect and tolerance of the selected part. The minimum required BPH pin capacitance is 2.6 µF assuming a maximum HS duty ratio of 100 % at 1 kHz as shown in Figure 13 (derived from data sheet).

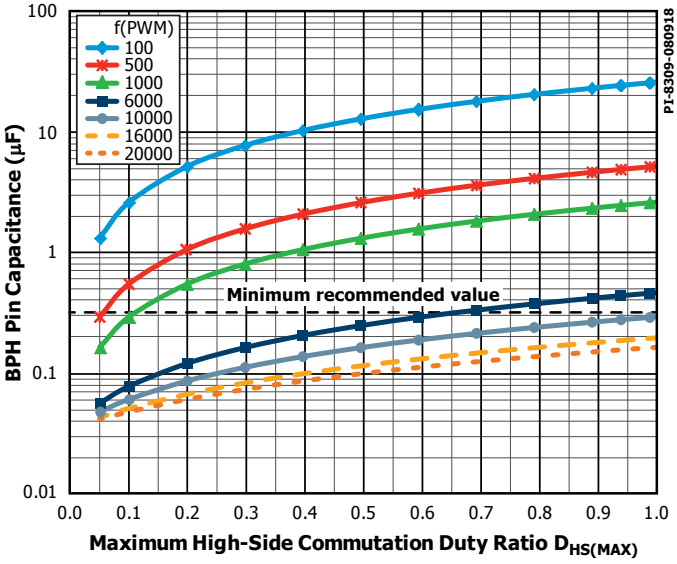


Figure 13. BYPASS HIGH-SIDE Pin Capacitance at 1 kHz High-Side Commutation PWM Frequency with 100 % Duty Ratio.

The selected part number is GRM31CR61E47KA88 (4.7 µF, 25 V, X5R, ±10%, 1206/1.8 mm). From the DC bias characteristic curve depicted in Figure 14, its capacitance will be reduced to 3.36 µF at 14.5 V. Assuming a -10% tolerance, the effective capacitance is 3.0 µF which satisfies the minimum 2.6 µF requirement.

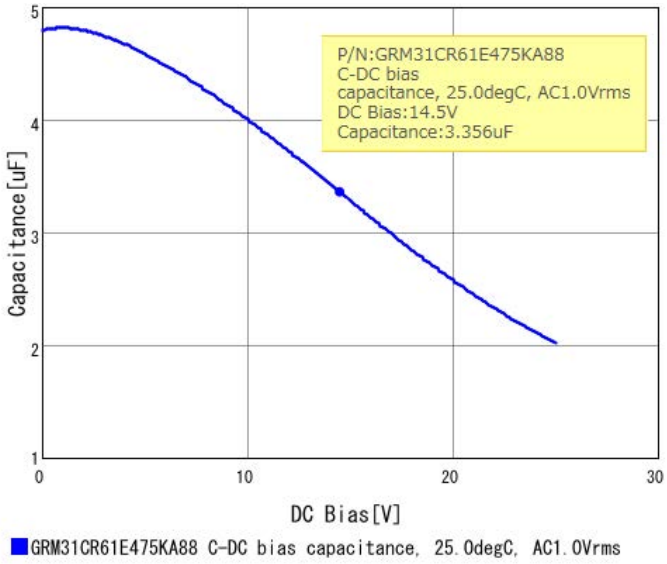


Figure 14. DC Bias Characteristic of GRM31CR61E47KA88 Multi-Layer Ceramic Capacitor.

Control input signals INL_U, /INH_U, INL_V and /INH_V, control the switching state of the integrated high-side and low-side power FREDFETs. These control input signals interface to the system micro-controller through pins 4, 5, 8 and 9 of the signal interface connector J2. Series resistors R11, R9, R12, and R10 maintain the signal integrity of the control input signals.

Resistors R14, R7, R16, and R8 set the cycle-by-cycle current limit level for the integrated low-side and high-side power FREDFETs of the two devices respectively. The selected value of 44.2 kΩ sets it to 100% of the default level. The default current limit, $I_{LIM(DEF)}$ = 0.7 A (typical) at di/dt = 250 mA/µs with BRD1260C device.

IPH pin outputs across resistors R13 and R15 provide the instantaneous phase current information of the low-side power FREDFET Drain to Source current of U1 and U2 devices respectively. With BRD1260C, the IPH pin output gain is 400 µA/A, and the selected RIPH value of 7.5 kΩ translates into a 3 V signal per 1 A drain current. The respective IPH pin output signals IPH_U and IPH_V of devices U1 and U2 are accessible on pins 3 and 7 of the signal interface connector J2.

Device U1 implements the DC bus line sensing through resistors R1, R2, and R3. Their combined resistance of 7 MΩ sets the under-voltage thresholds to 247 V, 212 V, 177 V, and 142 V provided in Table 2. The set bus overvoltage threshold is 422 V. The capacitor C6 provides optional high-frequency noise decoupling at the SM pin. On the other hand device U2 provides a system sense input exposing the SM pin externally through pin 6 of connector J2. This can be connected externally, for example to implement a system temperature sense through an external thermistor. Capacitor C5 provides optional high-frequency noise decoupling at the SM pin.

Each BridgeSwitch will report any detected internal and system fault through the status communication bus (FAULT bus) located on pin 2 of connector J2. The two FAULT pins of each BridgeSwitch device are tied together in a single wire bus using a pull-up resistor (i.e. 10 kΩ) to the VDD supply. The pull-up supply (VDD) for the open-drain fault output is available on pin 1 of the same connector. The device U1 ID pin is shorted to SG with t_{ID} of 80 µs and the device U2 ID pin is floating with t_{ID} of 60 µs. Application note AN-80 provides a detailed description of how to use the FAULT Communication Interface. It is available at www.power.com: https://motor-driver.power.com/products/bridgeswitch-family/bridgeswitch/

A 10-position connector header J2 interfaces the 1-phase inverter stage to the system micro-controller for the control inputs, instantaneous phase current information, external system sense input and the status communication bus.

The circuit also provides an external bias option to supply the integrated low-side driver through BPL pin of each BridgeSwitch device from a single input rail through the J3 connector. The optional external bias operation reduces the dissipation inside the package due to self-supply and addresses low inverter no-load input power, a requirement for some applications. Capacitor C2 provides local decoupling of the external DC supply. Resistors R4 and R5 limit the external supply current on the BPL pin to less than 12 mA (I_{SUP} = 1.5 mA to 2 mA recommended) for the respective BridgeSwitch devices. The chosen resistor value of 560 Ω assumes a 1.6 mA supply current given a maximum BPL pin shunt regulator voltage of 16.1 V and a 17 V external supply voltage. The limiting resistors must be depopulated when operating in self-supply mode to prevent BPL voltage threshold interactions.

Key Application Design Consideration

PCB Layout

The performance and reliability of the inverter are dependent on the printed circuit board (PCB) layout. The PCB layout guidelines described in this section employ the general guidelines specified in the data sheet for all BridgeSwitch designs. The following depicts the recommended layout illustrated on the DER-873 1-phase inverter board.

The BYPASS pin decoupling capacitors are placed as close as possible to the BridgeSwitch respective BPH and BPL pins in order to maximize noise immunity and to keep supply stability. The BPL decoupling capacitor returns directly to the SG pin and the BPH decoupling capacitor returns directly to the HB pin.

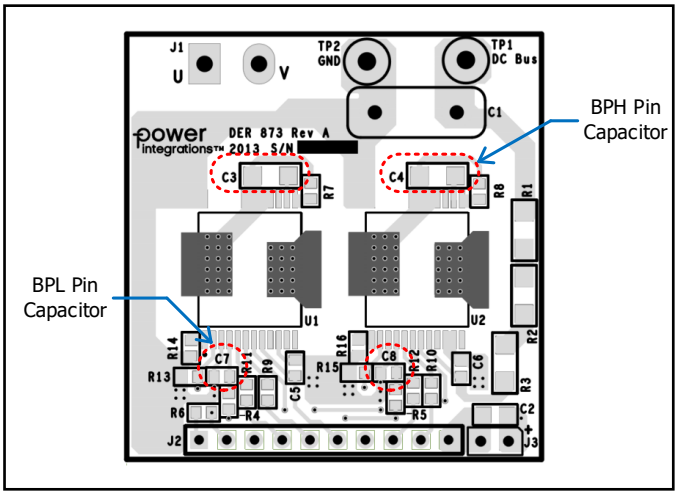


Figure 15. BPL Pin and BPH Pin Capacitors Layout Placement.

The XL pin resistor is placed as close as possible to the XL pin with reference to the SG pin. The XH resistor is placed as closed as possible to the XH pin with reference to the HB pin. This minimizes loop area for both current reference paths.

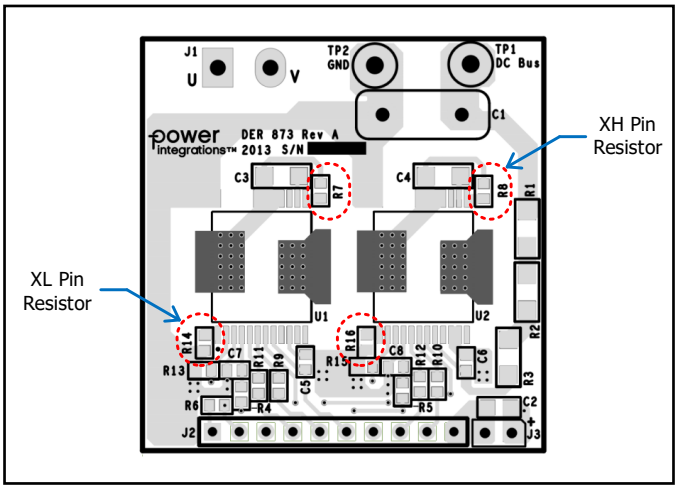


Figure 16. XL Pin and XH Pin Resistors Layout Placement.

The control input resistors are placed as close as possible to the respective INL and INH pins. In addition, if possible the PCB trace lengths carrying the control signals from the micro-controller should be minimized and placed far from any high-voltage switching traces.

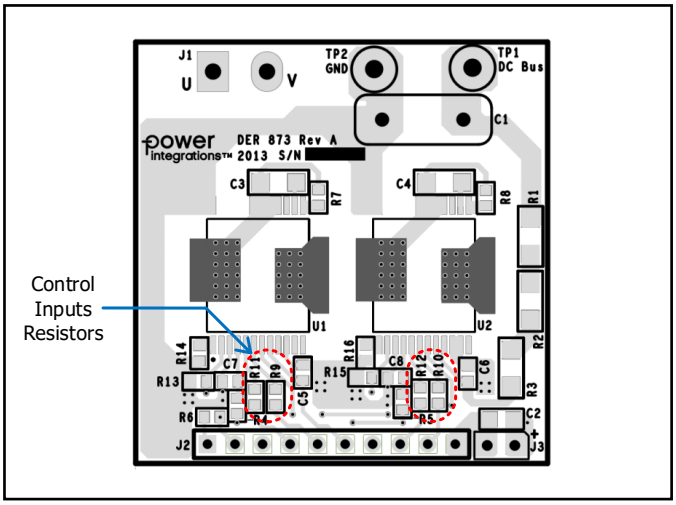


Figure 17. Control Inputs Resistor Layout Placement.

When the SM pin is configured as a DC bus line sense, the line-sense resistors are placed as close as possible to the IC with minimum trace lengths. Consequently, the optional filter capacitor is placed as close as possible to the SM pin and returns to the SG pin.

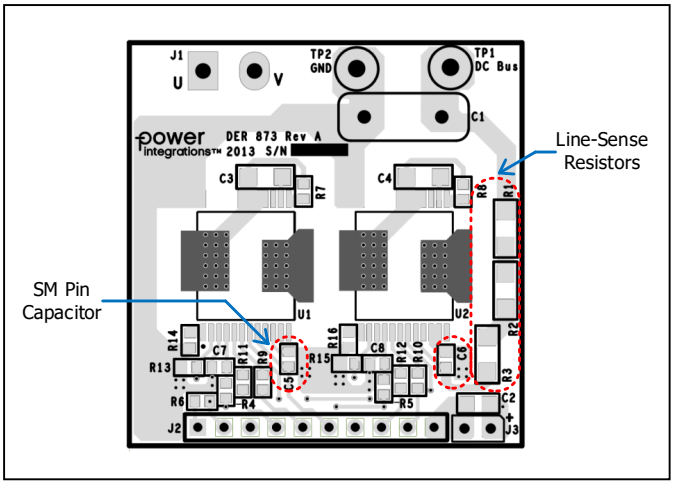


Figure 18. SM Pin Capacitor and Line-Sense Resistor Layout Placement.

The IPH resistor is placed as closed as possible to the IPH pin. The length of PCB traces carrying the IPH signal to the system micro-controller should be kept as short as possible to avoid noise pick up and maintain signal integrity. The IPH resistor refers to the SG pin.

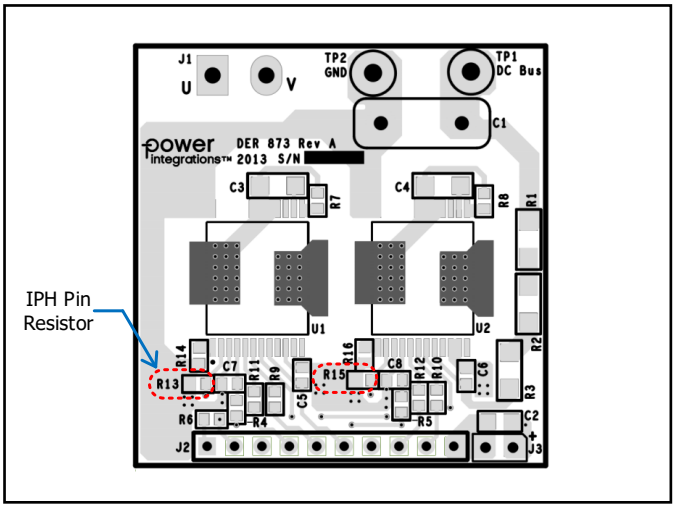


Figure 19. IPH Pin Resistor Layout Placement.

All low-side control circuits and system micro-controller signals refer to the signal ground (SG pin). The signal ground pins of each device are connected through a solid copper connection and connect directly to the low-side power FREDFET SOURCE pin (LS pin). The power ground is formed by the LS pin trace to the DC link capacitor return. A solid copper power ground plane is recommended.

The HD pin decoupling capacitor provides the inverter local decoupling of the DC bus voltage. The capacitor is placed as close as possible to the BridgeSwitch devices to minimize the loop area with the safety creepage and/or clearance requirement considered.

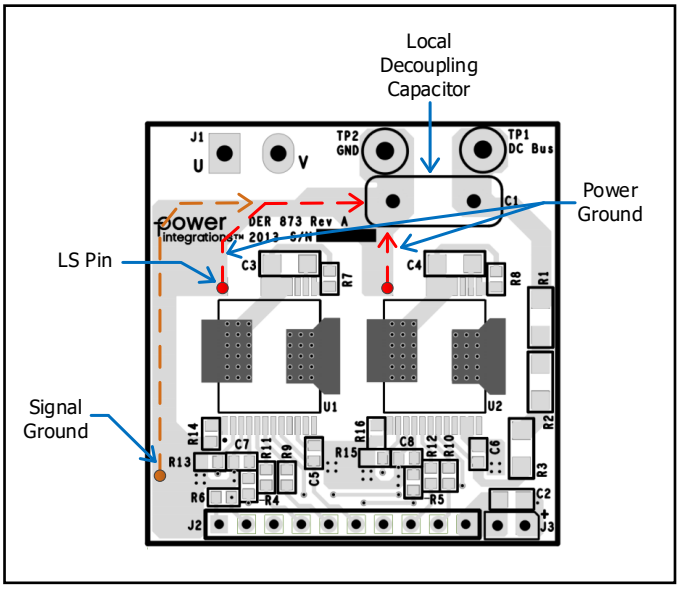


Figure 20. Local Decoupling and Ground Connection Layout.

Thermal Management

PCB layout plays an important role in the thermal performance of each BridgeSwitch device. BridgeSwitch InSOP-24C package exposed pads (HD and HB) facilitate effective heat transfer to the PCB eliminating the use of an external heat sink. The configuration and distance among devices, the area of the PCB copper clad connected to the exposed pad, and the copper thickness all impact thermal performance.

A BridgeSwitch whitepaper discusses specifically the "Impact of Printed Circuit Board Layout on Device Temperature in 3-phase Inverters Using BridgeSwitch" and can be downloaded at www.power.com: https://motor-driver.power.com/products/bridgeswitch-family/bridgeswitch/

Generally, best thermal performance is achieved by placing each BridgeSwitch device farther from each other and maximizing the copper thickness and available PCB area while ensuring no violation in any of the PCB design guidelines. However, in some practical applications limited PCB area is allowed for highly compact designs.

The DER-873 1-phase inverter board has excellent thermal performance considering a limited PCB space. It demonstrates less than 35 °C package temperature rise above ambient with BRD1260C at full load. The bottom layer PCB is utilized as the heat sink for each package accomplished through the use of thermal vias placed directly underneath the exposed pads. The thermal vias used have an outer diameter of 0.8 mm and an inner diameter of 0.5 mm. The printed board uses FR4 laminate with a copper thickness of 70 μm (610 g/m²).

Figure 21 depicts the DER-873 bottom layer PCB heat sinking including the HD and respective HB copper areas of each device as well as thermal via locations.

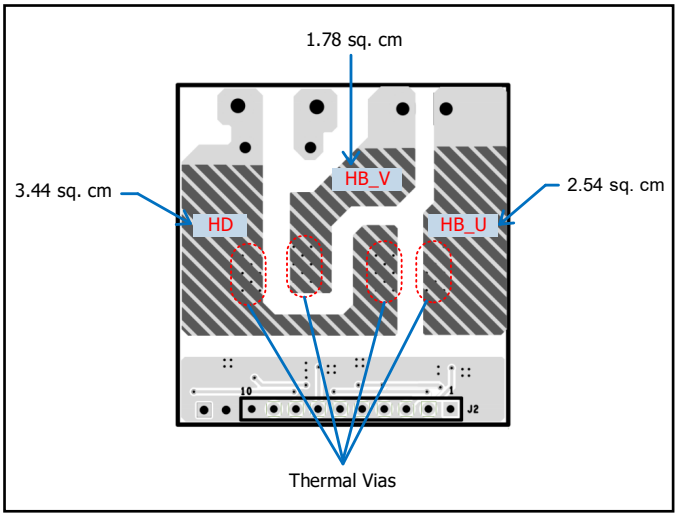


Figure 21. Bottom Layer PCB Heat Sinking.

Appendix

1-Phase Motor Control Strategies Software Control Implementation Example

This section provides an example software implementation of the square wave and the back-emf tailored control referred to in this document as "trapezoidal control". It presents an introduction to one example implementation of each control strategy mentioned with a Hall sensor.

Referring to the typical control software block diagram depicted in Figure 22, the implementation of each control strategy is handled by the commutation block within the inner loop, while the speed control is handled within the outer loop.

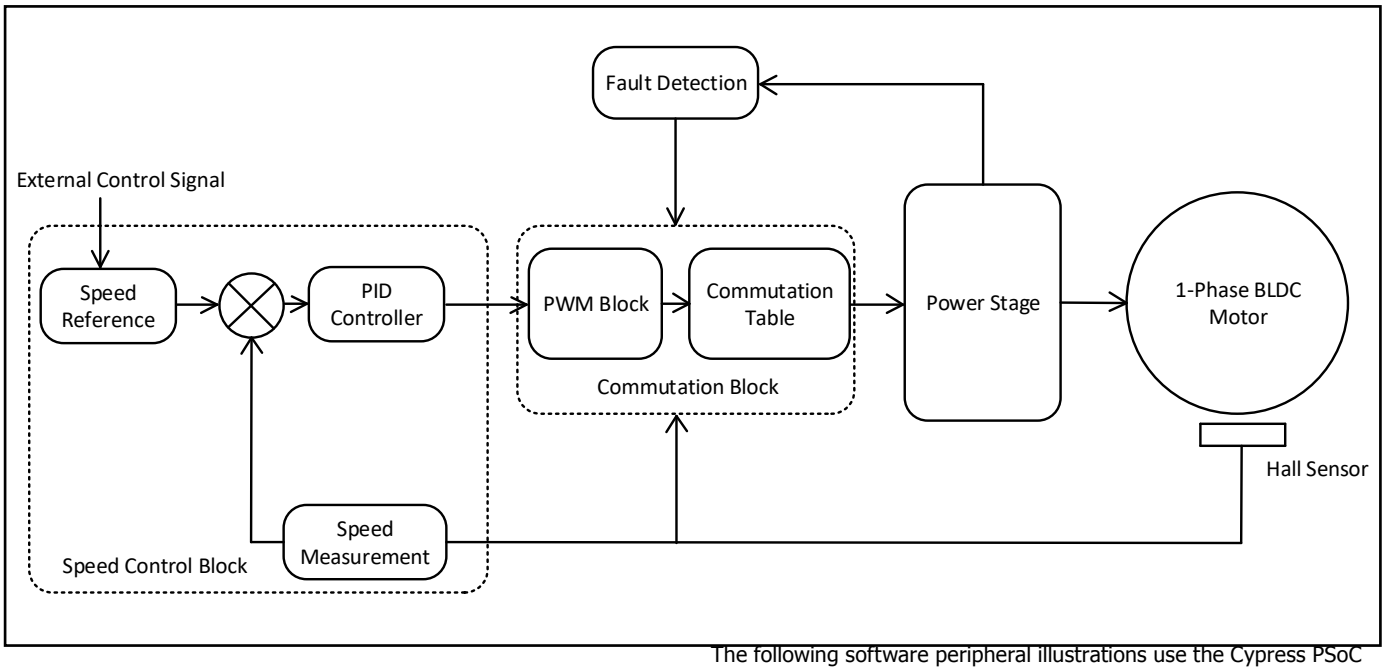


Figure 22. Typical 1-Phase BLDC Motor Control Software Block Diagram.

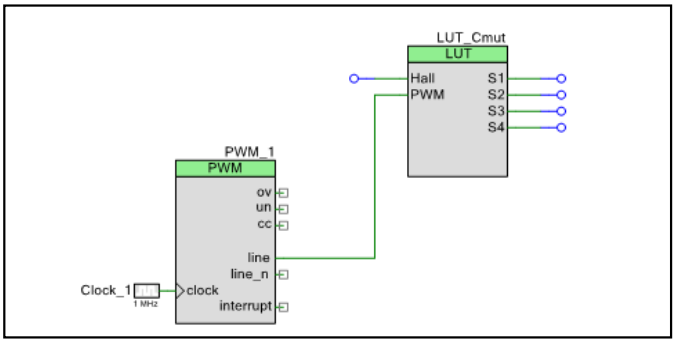
Square-Wave PWM-Based Control Implementation

The commutation block for square wave control contains a commutation control and PWM block typically implemented using a look up table (LUT).

The LUT is a simple truth table that translates the commutation sequence for one electrical cycle. It consists of two input states and four output states. The first input state is the hall sensor signal from the motor which provides rotor position feedback. The second input state is the PWM control. In this implementation, it toggles the respective high-side switch ON/OFF to control the motor speed with the duty cycle commanded by the speed control block. The four output states are the control signals to the respective transistor switches of the full bridge inverter.

Figure 23 depicts the PWM and LUT software peripherals used in this example. The commutation table described below will generate the exact commutation timing diagram depicted in Figure 8.

The following software peripheral illustrations use the Cypress PSoC Creator IDE version 4.1.



Input Hex Value	PWM	Hall		S4	S3	S2	S1	Output Hex Value
00	0	0		0	0	1	0	0x02
01	0	1		1	0	0	0	0x08
02	1	0		0	1	1	0	0x06
03	1	1		1	0	0	1	0x09

Figure 23. Software Peripheral Blocks and LUT for Square Wave Control.

Trapezoidal Control Implementation

For the trapezoidal control implementation, the principle relies on the application of a drive current that resemble the shape of the motor back-emf. In principle, it produces the ideal torque for the motor and reduces the overall harmonic distortion compared to square-wave control. Figure 24 depicts an example back-emf shape of a 1-phase motor.

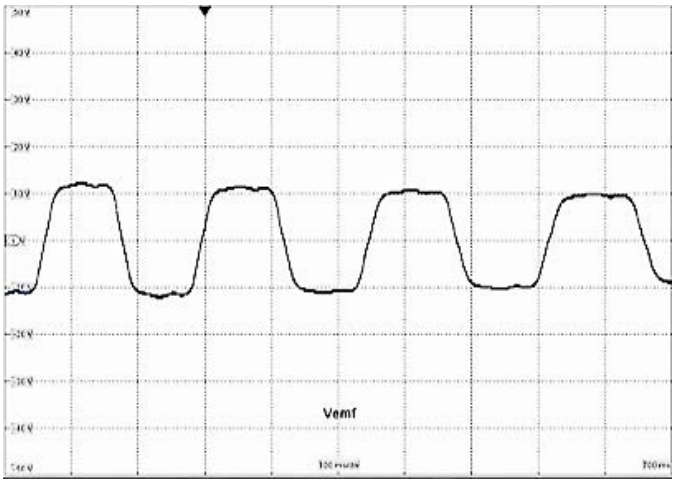


Figure 24. Back-emf Shape of a 1-Phase BLDC Motor.

For this type of control, the commutation implementation is the same with square wave control except that the PWM duty cycle is modulated to produce the desired wave shape. Figure 25 depicts the commutation timing diagram showing an example modulation on the high-side control signals.

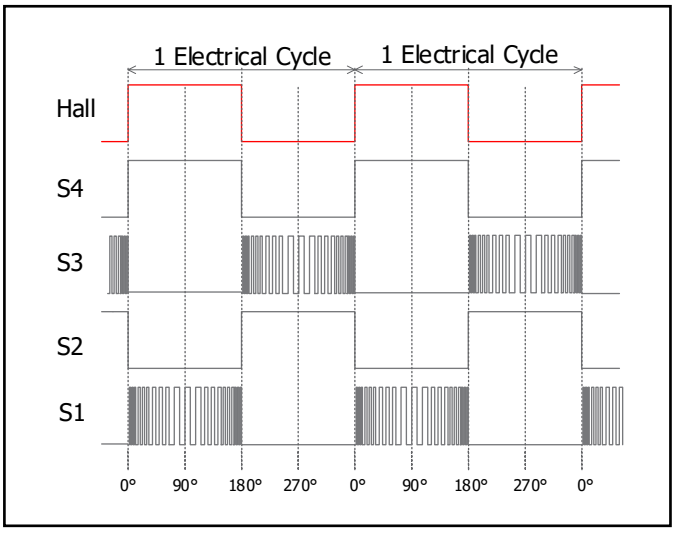


Figure 25. Commutation Timing Diagram with Duty Cycle PWM Modulation.

The conventional approach for creating the desired wave shape with PWM is through the use of a look up table (LUT). The LUT is accomplished through the use of an array containing duty cycle values as its elements. The number of elements in the LUT will decide the number of sample points to create the desired wave shape. The higher the number of sample points the lower the quantization error. Only half-wave modulation is required during each commutation (0° – 180° and 180° – 360° intervals); hence, a half-wave LUT is used.

Figure 26 depicts an overview of the trapezoidal PWM generation using a LUT. The LUT timer block decides the sampling of the LUT. The PWM duty cycle varies every time the timer generates an interrupt. Each time an interrupt is generated, a duty cycle is assigned to the next value in the LUT. The interval at which the timer generates the interrupt is the sampling time. Figure 27 depicts an example PWM duty cycle pattern implemented in the software in a 12-bit LUT.

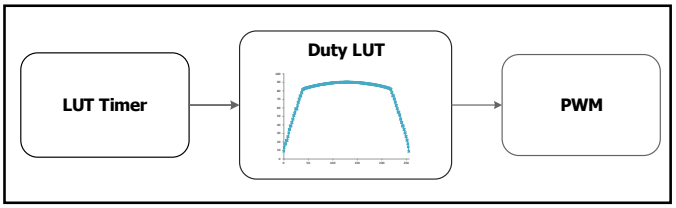


Figure 26. Trapezoidal PWM Duty Cycle Generation Overview.

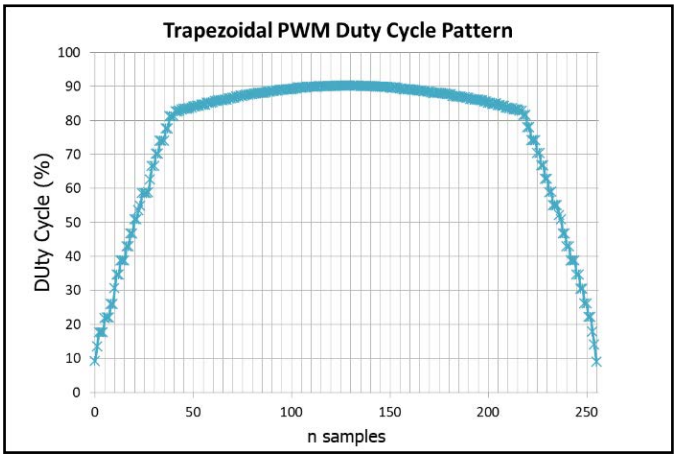


Figure 27. Trapezoidal PWM Duty Cycle Pattern.

Below is a code snippet illustrating the writing of the LUT duty cycle value to the PWM component every sampling period of the timer block.

```
if(interrupt == INTERRUPT_OCCURED){

     /*Change duty cycle of PWM at the end of each interrupt*/
     PWM_1_WriteCompare(look_up[position++]);

     }

if(position>255){

     /*When array limit is exceeded in LUT (i.e 12-bit LUT),
      roll back to position 0*/

     position = 0;}

     }

/*Clear interrupt*/
ClearInterrupt();
```

The sampling time of the LUT to create trapezoidal wave modulation is set to match the period of the motor's electrical speed. In this case, a second timer (Hall Timer) is used to measure the motor's electrical speed using the hall sensor signal information. In the same manner, the measured electrical speed by the Hall Timer is fed to the speed control block for speed regulation.

Figure 28 depicts the software peripherals used in this implementation. Two timer peripherals are added (LUT Timer and Hall Timer) to the original square-wave software peripheral blocks.

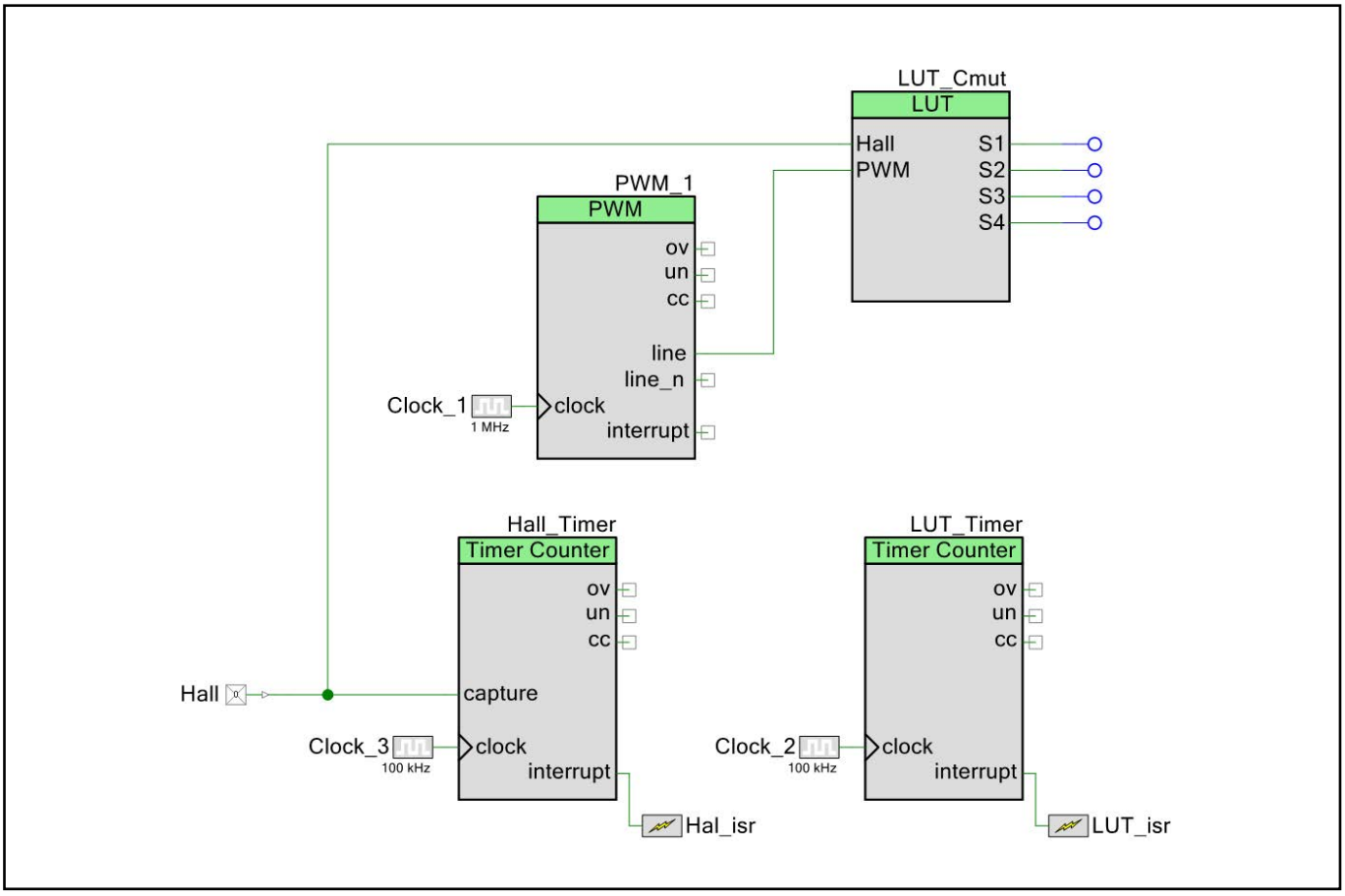


Figure 28. Software Peripheral Blocks for Trapezoidal Control.

Notes

Revision	Notes	Date
A	Initial release.	06/20

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