Design Example Report

Title	***30 W USB PD 3.0 Power Supply with 3.3 V – 21 V PPS Output Using InnoSwitch™ 3-Pro PowiGaN™ INN3378C-H302 and VIA Labs VP302 Controller***
Specification	90 VAC – 265 VAC Input; 5 V / 3 A, 9 V / 3 A, 15 V / 2 A, 20 V / 1.5 A, 3.3 V – 11 V / 3 A PPS (30 W Power-limited), or 3.3 V – 21 V / 1.5 A PPS (30 W Power-limited) Output
Application	USB PD / PPS Power Adapter
Author	Applications Engineering Department
Document Number	DER-908
Date	September 19, 2020
Revision	1.3

Summary and Features

- InnoSwitch3-Pro - digitally controllable CV/CC QR flyback switcher IC with integrated high-voltage MOSFET, synchronous rectification and FluxLink™ feedback
    - I^{2}C Interface enables low pin count USB PD Controller VP302 (8 pin)
    - Sophisticated telemetry and comprehensive protection features
- Meets DOE6 and CoC v5 2016 Average Efficiency requirements with high margin (>3.0%)
    - 5 V Output: 91.00% at 115 VAC (9.16% margin); 89.62% at 230 VAC (7.79% margin)
    - 9 V Output: 91.93% at 115 VAC (4.63% margin); 91.51% at 230 VAC (4.22% margin)
    - 15 V Output: 91.95% at 115 VAC (4.25% margin); 91.73% at 230 VAC (4.03% margin)
    - 20 V Output: 91.22% at 115 VAC (3.52% margin); 90.99% at 230 VAC (3.29% margin)
- <20 mW no-load input power at 230 VAC
- Meets CISPR22 / EN55022 Class B Conducted EMI with high margin
    - >3dB margin at worst case condition (20 V / 1.5 A, 230 VAC)
- Low component count, high power density
    - Total part count: 59
    - Power density: 9.66 W / inch^3 without enclosure (1.87″ x 1.77″ x 0.94″ form factor)

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PATENT INFORMATION

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.power.com. Power Integrations grants its customers a license under certain patent rights as set forth at https://www.power.com/company/intellectual-property-licensing/.

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Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This document is an engineering report describing a 30 W USB PD 3.0 power supply using InnoSwitch3-Pro INN3378-H302 IC and VIA Labs VP302 USB PD controller. The USB PD source capabilities of the power supply are listed below.

- PDO1: 5 V / 3 A (Fixed Supply)
- PDO2: 9 V / 3 A (Fixed Supply)
- PDO3: 15 V / 2 A (Fixed Supply)
- PDO4: 20 V / 1.5 A (Fixed Supply)
- PDO5: 3.3 V – 11 V / 3 A (Programmable Power Supply, 30 W power-limited)
- PDO6: 3.3 V – 21 V / 1.5 A (Programmable Power Supply, 30 W power-limited)

This design shows the high power density and efficiency that is possible due to the high level of integration of the InnoSwitch3-Pro controller providing exceptional performance.

The report contains the power supply specification, schematic diagram, printed circuit board layout, bill of materials, magnetics specifications, and performance data.

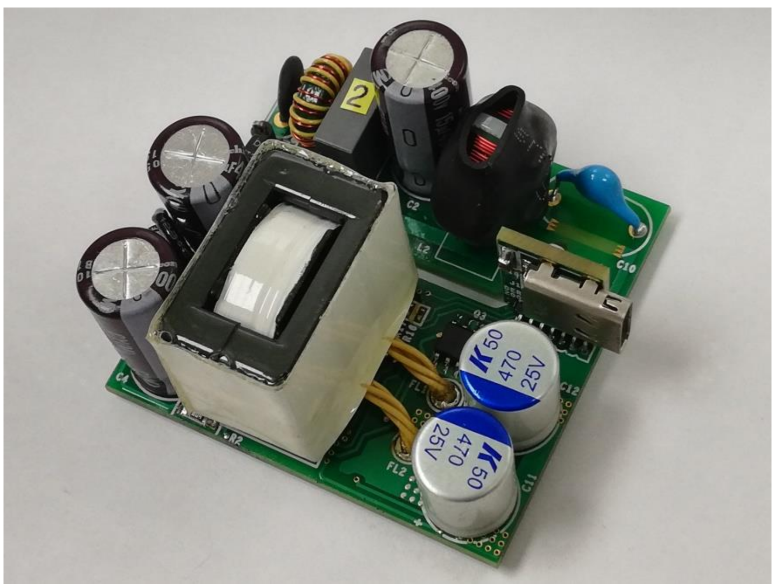

Figure 1 – Populated Circuit Board Photograph, Entire Assembly.

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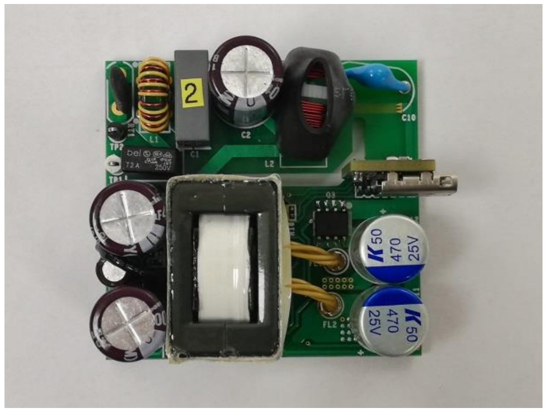

Figure 2 – Populated Circuit Board Photograph - Top.

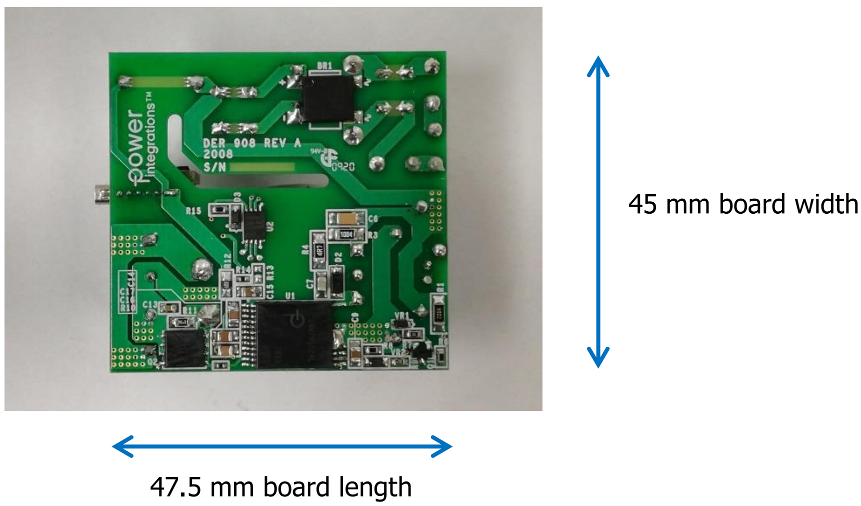

Figure 3 – Populated Circuit Board Photograph - Bottom.

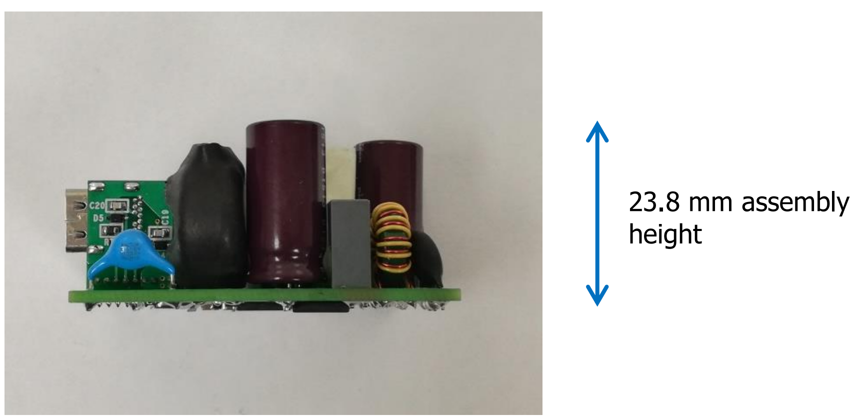

Figure 4 – Populated Circuit Board Photograph - Side.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power				20	mW	Measured at 230 VAC
5 V / 3 A Setting						
Output Voltage	$V_{OUT(5 V)}$		5.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(5 V)}$			150	mV	Measured at End of 100 mΩ Cable.
Output Current	$I_{OUT(5 V)}$			3.0	A	±3%
Average Efficiency	$\eta_{(5 V)}$	90.5			%	Measured at 115 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(5 V)}$			15	W	
9 V / 3 A Setting						
Output Voltage	$V_{OUT(9 V)}$		9.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(9 V)}$			150	mV	Measured at End of 100 mΩ Cable.
Output Current	$I_{OUT(9 V)}$			3.0	A	±3%
Average Efficiency	$\eta_{(9 V)}$	91.4			%	Measured at 115 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(9 V)}$			27	W	
15 V / 2 A Setting						
Output Voltage	$V_{OUT(15 V)}$		15.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(15 V)}$			150	mV	Measured at End of 100 mΩ Cable.
Output Current	$I_{OUT(15 V)}$			2.0	A	±3%
Average Efficiency	$\eta_{(15 V)}$	91.4			%	Measured at 115 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(15 V)}$			30	W	
20 V / 1.5 A Setting						
Output Voltage	$V_{OUT(20 V)}$		20.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(20 V)}$			150	mV	Measured at End of 100 mΩ Cable.
Output Current	$I_{OUT(20 V)}$			1.5	A	±3%
Average Efficiency	$\eta_{(20 V)}$	90.7			%	Measured at 115 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(20 V)}$			30	W	
3.3 V – 11 V PPS Setting						
Maximum Programmable Output Voltage	$V_{OUT,MAX}$			11	V	APDO Maximum Voltage.
Minimum Programmable Output Voltage	$V_{OUT,MIN}$	3.3			V	APDO Minimum Voltage.
Output Current	$I_{OUT,PPS}$			3.0	A	±3%
PPS Voltage Step	$V_{STEP,PPS}$		20		mV	PPS Voltage Step (USB PD 3.0).
PPS Current Step	$I_{STEP,PPS}$		50		mA	PPS Current Step (USB PD 3.0).
Continuous Output Power	P_{OUT}			30	W	PPS Power Limited bit = 1 (USB PD 3.0).

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3.3 – 21 V PPS Setting						
Maximum Programmable Output Voltage	$V_{OUT,MAX}$			21	V	APDO Maximum Voltage.
Minimum Programmable Output Voltage	$V_{OUT,MIN}$	3.3			V	APDO Minimum Voltage.
Output Current	$I_{OUT,PPS}$			1.5	A	±3%
PPS Voltage Step	$V_{STEP,PPS}$		20		mV	PPS Voltage Step (USB PD 3.0).
PPS Current Step	$I_{STEP,PPS}$		50		mA	PPS Current Step (USB PD 3.0).
Continuous Output Power	P_{OUT}			30	W	PPS Power Limited bit = 1 (USB PD 3.0).
Conducted EMI		Meets CISPR22B / EN55022B				
Ambient Temperature	T_{AMB}	0		40	ºC	Open Frame, Sea Level.

Note: To use this design for a charger/adapter with a different shape and form factor, the changes in the circuit board layout must be carefully evaluated to meet the target specifications for EMI, ESD, and Line Surge performance.

3 Schematic

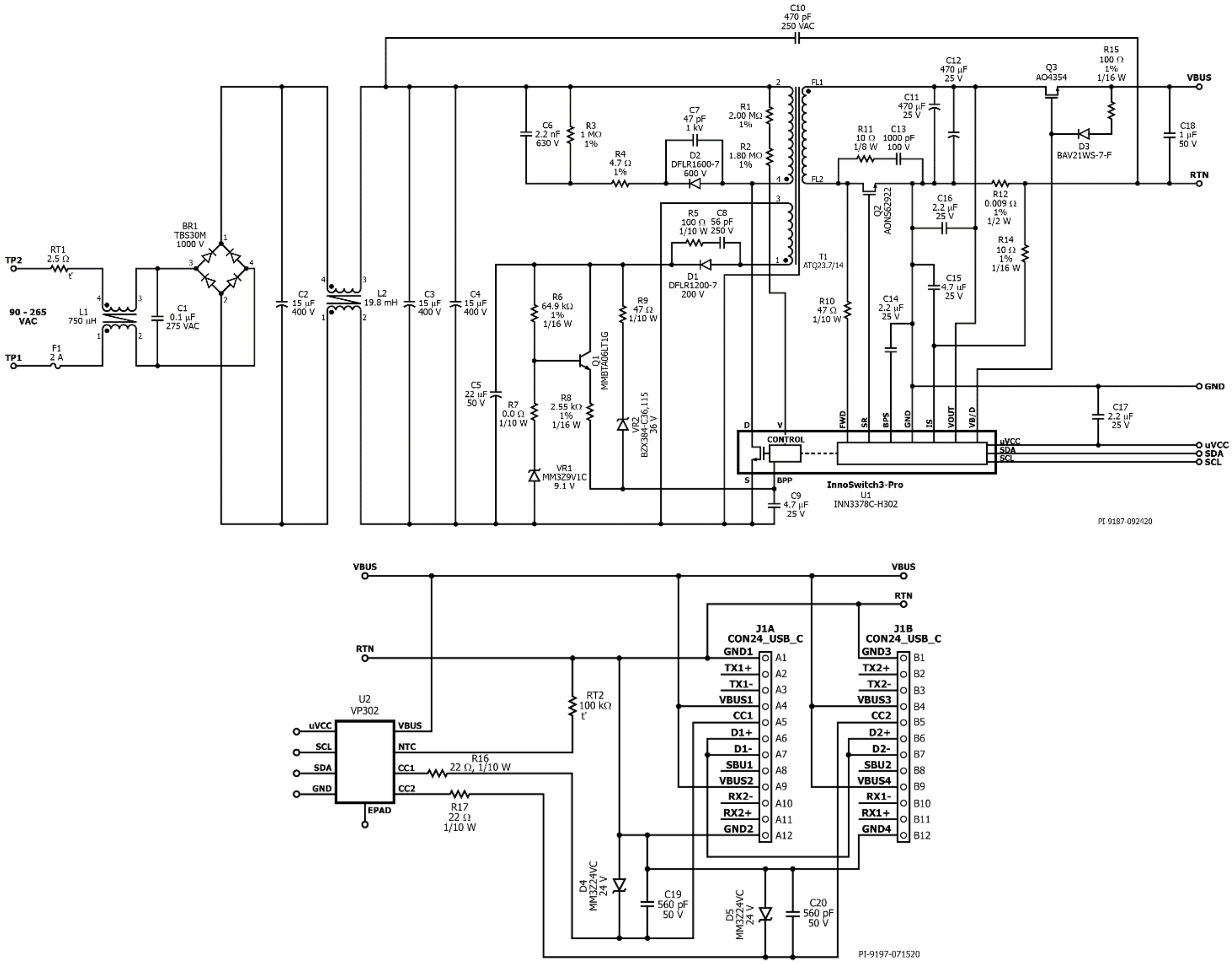

Figure 5 –Schematic.

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4 Circuit Description

4.1 *Input Rectifier and EMI Filter*

The input fuse F1 isolates the circuit and provides protection from component failure. NTC thermistor RT1 limits the inrush current when the input AC supply is connected. Common mode chokes L1 and L2, with capacitors C10 and C1 provide common mode and differential mode noise filtering for EMI attenuation. Bridge rectifier BR1 rectifies the AC line voltage to have a full wave rectified DC, which is filtered by the bulk capacitors C2, C3, and C4.

4.2 *InnoSwitch3-Pro IC Primary*

One end of the flyback transformer T1 primary winding is connected to the rectified DC bus and the other end is connected to the drain terminal of the switch inside the InnoSwitch3-Pro IC U1. Resistors R1 and R2 provide input voltage sensing for protection in case of AC input undervoltage or overvoltage.

A low-cost R2CD clamp formed by diode D2, resistors R3, and R4, and capacitor C6 limits the peak drain-source voltage of U2 at the instant the switch inside U2 turns off. The clamp helps to dissipate the energy stored in the leakage reactance of transformer T1. Capacitor C7 provides damping of high frequency ringing in the voltage across diode D2 to reduce radiated EMI.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor C9 when AC is first applied. During normal operation, the primary side block is powered from an auxiliary winding on the transformer T1. The output of the auxiliary (or bias) winding is rectified using diode D1 and filtered using capacitor C5. Resistor R8 limits the current being supplied to the BPP pin of the InnoSwitch3-Pro IC U1. A linear regulator comprising resistor R6, R7, BJT Q1 and Zener diode VR1 ensures sufficient current flows through R8 such that the internal current source of U1 is not required to charge C9 during normal operation. The RC network consisting of resistor R5 and capacitor C8 offers damping of the high frequency ringing in the voltage across diode D1 to reduce radiated EMI.

Zener diode VR2 offers primary sensed output overvoltage protection. In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In case of overvoltage at output of the converter, the auxiliary winding voltage increases and causes breakdown of VR2 which then causes excess current to flow into the BPP pin of InnoSwitch3-Pro IC U1. If the current flowing into the BPP pin increases above the I_{SD} threshold, the InnoSwitch3-Pro controller will latch off and prevent any further increase in output voltage. Resistor R9 limits the current injected to BPP pin when the output overvoltage protection is triggered.

4.3 *InnoSwitch3-Pro IC Secondary and USB Power Delivery Controller*

The secondary-side of the InnoSwitch3-Pro IC provides output voltage and current sensing and a gate drive to a FET for synchronous rectification. The voltage across the transformer secondary winding is rectified by the secondary-side synchronous rectifier FET (SR FET) Q2 and filtered by capacitors C11 and C12. High frequency ringing during switching transients that would otherwise create radiated EMI is reduced via a RC snubber, R11 and C13.

The gate of Q2 is turned on by secondary-side controller inside IC U1, based on the secondary winding voltage sensed via resistor R10 and fed into the FWD pin of the IC.

In continuous conduction mode of operation, the SR FET is turned off just prior to the secondary-side commanding a new switching cycle from the primary. In discontinuous mode of operation, the SR FET is turned off when the magnitude of the voltage drop across the SR FET falls below a threshold of approximately $V_{SR(TH).}$ Secondary-side control of the primary-side power switch avoids any possibility of cross conduction of the two switches and provides extremely reliable synchronous rectifier operation.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. Capacitor C14 connected to the BPS pin of InnoSwitch3-Pro IC U1 provides decoupling for the internal circuitry.

The output current is sensed by monitoring the voltage drop across resistor R12. The current measurement is filtered with decoupling capacitor C15 and monitored across the IS and SECONDARY GROUND pins. An internal current sense threshold which is configured via the I^2C interface up to approximately 32 mV is used to reduce losses. Once the threshold is exceeded, the InnoSwitch3-Pro IC U2 regulates the number of switch pulses to maintain a fixed output current.

During constant current (CC) operation, when the output voltage falls, the secondary side controller inside InnoSwitch3-Pro IC U1 will power itself from the secondary winding directly. During the on-time of the primary-side power switch, the forward voltage that appears across the secondary winding is used to charge the SECONDARY BYPASS pin decoupling capacitor C14 via resistor R10 and an internal regulator. This allows output current regulation to be maintained down to the minimum UV threshold. Below this level the unit enters auto-restart until the output load is reduced.

When the output current is below the CC threshold, the converter operates in constant voltage mode. The output voltage is monitored by the VOUT pin of the InnoSwitch3-Pro IC. Similar with current regulation, the output voltage is also compared to an internal voltage threshold that is set via the I^2C interface and the controller inside IC U1 regulates the output voltage by controlling the number of switch pulses. Capacitor C16 is needed between the VOUT pin and the SECONDARY GROUND pin for ESD protection of the VOUT pin.

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N-channel MOSFET Q3 functions as the bus switch which connects or disconnects the output of the flyback converter from the USB Type-C receptacle. MOSFET Q3 is controlled by the VB/D pin on the InnoSwitch3-Pro IC. Resistor R15 and diode D3 are connected across the Source and Gate terminals of the Q2 to provide a discharge path for the bus voltage when the Q3 is turned off. Capacitor C18 is used at the output for ESD protection and output voltage ripple reduction.

In this design, VP302 (U2) is the USB Power Delivery (USB PD) controller. It is powered by the InnoSwitch3-Pro IC through the µVCC pin. USB PD protocol is communicated over either CC1 or CC2 line depending on the orientation in which Type-C plug is connected.

VP302 communicates with InnoSwitch3-Pro IC through the I^2C interface using the SCL and SDA lines in which it sets the CV, CC, V_{KP}, OVA and UVA parameters. These parameters correspond to the output voltage, constant output current, constant output power voltage threshold, output overvoltage threshold, and output undervoltage threshold registers of the InnoSwitch3-Pro IC, respectively. The status of the InnoSwitch3-Pro IC is read by the VP302 IC from the telemetry registers also using the I^2C interface.

Capacitor C17 provides decoupling to the µVCC of the InnoSwitch3-Pro IC and VCC of the VP302 IC. Capacitors C19 and C20, resistors R16 and R17, and zener diodes D4, and D5 provide protection from ESD to pins CC1 and CC2.

Thermistor RT2 is connected to NTC pin of the VP302 IC to provide temperature detection of the USB Type-C receptacle. The VBUS pin of the VP302 IC is used to sense the output voltage at the USB Type-C receptacle, which is the voltage after the bus switch Q3. The VBUS pin is also used for discharging the capacitor C18 when the bus switch Q3 is opened.

5 PCB Layout

PCB copper thickness is 0.062 inches.

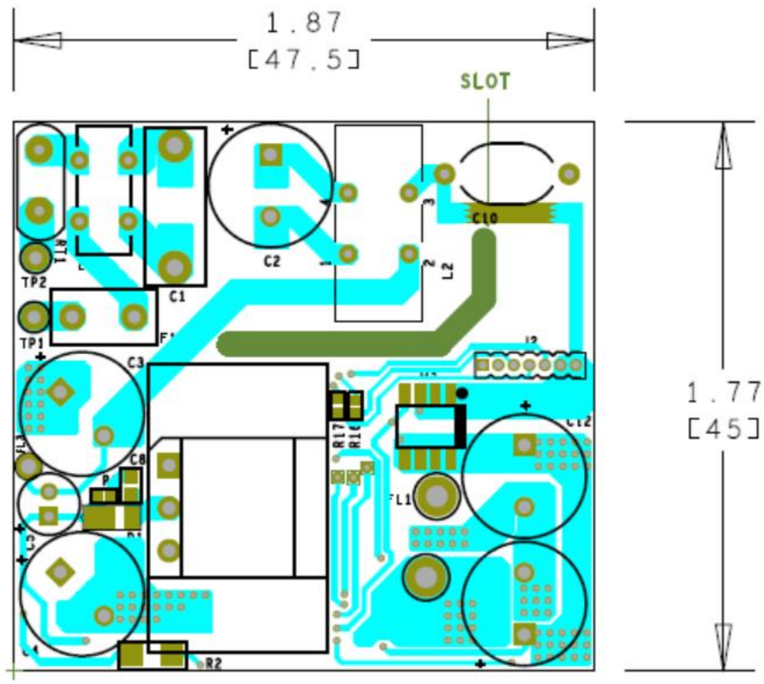

Figure 6 – DER-908 RevA PCB Layout, Top.

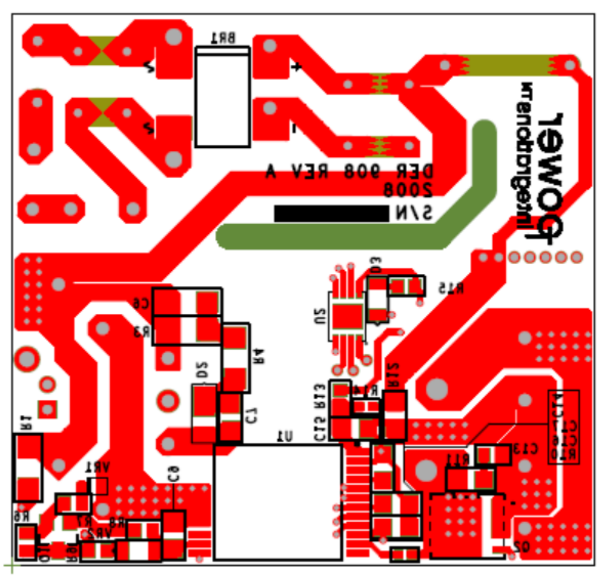

Figure 7 – DER-908 RevA PCB Layout, Bottom.

Note: Component references R13 and J2, although present in the layout, should not be populated.

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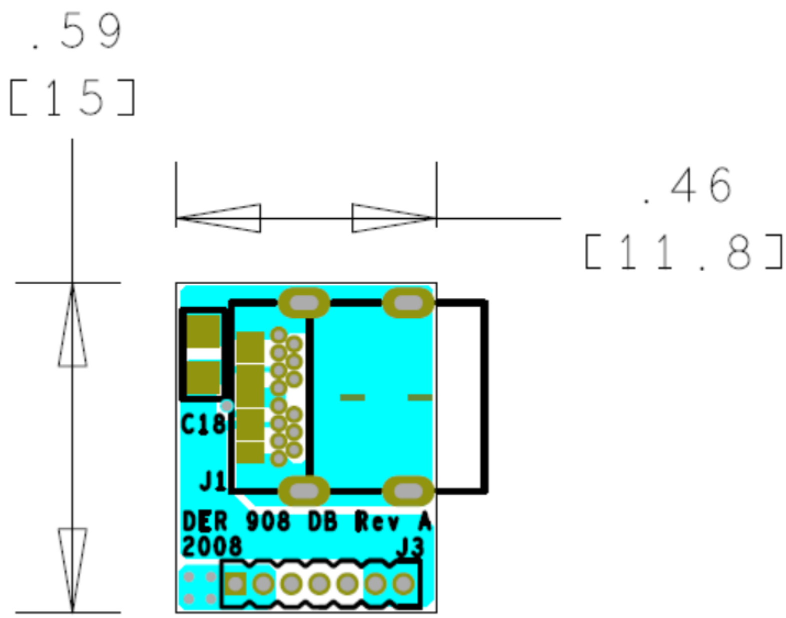

Figure 8 – USB Type-C Connector PCB Layout, Top.

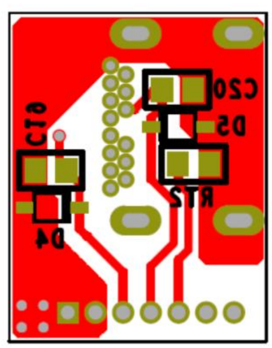

Figure 9 – USB Type-C Connector PCB Layout, Bottom.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	Bridge Rectifier Single Phase Standard 1 kV Surface Mount 4-TBS	TBS30M	Micro Commercial
2	1	C1	0.1 μF, 20% , 275VAC, 560VDC, X2, -40°C ~ 110°C, 5 mm W x 13 mm L x 11.1 mm H	R46KF310000P1M	KEMET
3	1	C2	15 μF, 400 V, Electrolytic, (10 x 20),	UCY2G150MPD	Nichicon
4	1	C3	15 μF, 400 V, Electrolytic, (10 x 20),	UCY2G150MPD	Nichicon
5	1	C4	15 μF, 400 V, Electrolytic, (10 x 20),	UCY2G150MPD	Nichicon
6	1	C5	22 μF, 50 V, Electrolytic, (5 x 11)	UPW1H220MDD	Nichicon
7	1	C6	2.2 nF, 630 V, Ceramic, X7R, 1206	C3216X7R2J222K	TDK
8	1	C7	47 pF, 1000 V, Ceramic, NP0, 0805	VJ0805A470JXGAT5Z	Vishay
9	1	C8	56 pF, 250 V, Ceramic, NP0, 0603	GQM1875C2E560JB12D	Murata
10	1	C9	4.7 μF, ±10%, 25 V, Ceramic, X7R, -55°C ~ 125°C, 0805	TMK212AB7475KG-T	Taiyo Yuden
11	1	C10	470pF, ±10%, 250VAC, X1, Y1, Ceramic Capacitor, B, Radial, Disc	DE1B3RA471KA4BN01F	Murata
12	1	C11	470 μF, 25 V,±20%, Al Organic Polymer, Gen. Purpose, Can, 15 mΩ, 2000 Hrs @ 105°C	A750MS477M1EAAE015	KEMET
13	1	C12	470 μF, 25 V,±20%, Al Organic Polymer, Gen. Purpose, Can, 15 mΩ, 2000 Hrs @ 105°C	A750MS477M1EAAE015	KEMET
14	1	C13	1000 pF, ±10%, 100 V, Ceramic, X7R, 0603	C0603C102K1RACTU	Kemet
15	1	C14	2.2 μF, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK
16	1	C15	4.7 μF, ±10%, 25 V, Ceramic, X7R, -55°C ~ 125°C, 0805	TMK212AB7475KG-T	Taiyo Yuden
17	1	C16	2.2 μF, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK
18	1	C17	2.2 μF, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK
19	1	C18	1 μF,±20% ,50 V, Ceramic, X7R, Boardflex Sensitive, 0805	CGA4J3X7R1H105M125AE	TDK
20	1	C19	560 pF, 50V, Ceramic, X7R, 0603 (1608 Metric), 0.063" L x 0.031" W (1.60mm x 0.80mm)	CC0603KRX7R9BB561	Yageo
21	1	C20	560 pF, 50V, Ceramic, X7R, 0603 (1608 Metric), 0.063" L x 0.031" W (1.60mm x 0.80mm)	CC0603KRX7R9BB561	Yageo
22	1	D1	200 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1200-7	Diodes, Inc.
23	1	D2	600 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1600-7	Diodes, Inc.
24	1	D3	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
25	1	D4	DIODE, ZENER, 24 V, 200 mW, SC-90, SOD-323F	MM3Z24VC	ON Semi
26	1	D5	DIODE, ZENER, 24 V, 200 mW, SC-90, SOD-323F	MM3Z24VC	ON Semi
27	1	F1	2 A, 250V, Slow, Long Time Lag, RST	RST 2	Belfuse
28	1	J1	Connector, "Certified", USB - C, USB 3.1, For 0.062" PCB Material, Superspeed+, Receptacle Connector, 24 Position, Surface Mount, Right Angle, Through Hole	632723300011	Wurth
29	1	J3	8 Position (1 x 8) header, 0.050" (1.27mm) pitch, Gold, R/A	M50-3930842	Harwin
30	1	L1	CMC, 750 μH @ 100 kHz, ±10%, Toroidal, wound on 32-00330-00 toroidal core	32-00403-00	Power Integrations
31	1	L2	Toroidal Common Mode Choke, 19.8 mH, ±25%, leakage inductance =100 μH max, DER-908, wound on 32-00286-00 core (14.90 mm O.D. 6.5 mm Th 7.0 mm ID)	32-00402-00	Power Integrations
32	1	Q1	NPN, Small Signal BJT, 80 V, 0.5 A, SOT-23	MMBTA06LT1G	On Semi
33	1	Q2	MOSFET, N-CH, 120V, 85A (at VGS=10V), Trench Power AlphaSGT 120V TM technology, DFN5X6	AONS62922	Alpha & Omega Semic
34	1	Q3	MOSFET, N-CH, 30 V, 23A (Ta), 3.1W (Ta),3.7 mΩ (@ 20 A, 10 V), 8SOIC MOSFET, N-CH, 30 V, 20A (Ta), 3.1W (Ta),5.8 mΩ (@ 20 A, 10 V), 8SOIC (alternate)	AO4354 AO4576	Alpha & Omega Semi
35	1	R1	RES, 2.00 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic

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36	1	R2	RES, 1.80 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1804V	Panasonic
37	1	R3	RES, 1.00 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1004V	Panasonic
38	1	R4	RES, 4.7 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8RQF4R7V	Panasonic
39	1	R5	RES, 100 Ω, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ101X	Panasonic
40	1	R6	RES, 64.9 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF6492V	Panasonic
41	1	R7	RES, 0 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEY0R00V	Panasonic
42	1	R8	RES, 2.55 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2551V	Panasonic
43	1	R9	RES, 47 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
44	1	R10	RES, 47 Ω, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ470X	Panasonic
45	1	R11	RES, 10 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ100V	Panasonic
46	1	R12	RES, 0.009 Ω, ±1%, 0.5 W, 0805, Current Sense, Moisture Resistant, Metal Element	CRF0805-FZ-R009ELF	Bourns
47	1	R14	RES, 10 Ω, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF10R0X	Panasonic
48	1	R15	RES, 100 Ω, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1000V	Panasonic
49	1	R16	RES, 22 Ω, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ220X	Panasonic
50	1	R17	RES, 22, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ220X	Panasonic
51	1	RT1	NTC Thermistor, 2.5 Ω, 3 A	SL08 2R503	Ametherm
52	1	RT2	NTC Thermistor, 100 kΩ, 1%, 4250K, 0603 (1608 Metric)	NCU18WF104F60RB	Murata
53	1	T1	Custom, DER-908 Transformer ATQ23.7-14, Lp = 425 μH		Power Integrations
54	1	TP1	Test Point, WHT, Miniature THRU-HOLE MOUNT	5002	Keystone
55	1	TP2	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone
56	1	U1	InnoSwitch3-Pro, InSOP24D	INN3378C-H302	Power Integrations
57	1	U2	IC, USB PD Type-C Controller for SMPS, DFN-8	VP302	VIA Labs
58	1	VR1	DIODE, ZENER, 9.1 V, 200mW, SC-90, SOD-323F	MM3Z9V1C	ON Semi
59	1	VR2	DIODE ZENER 36V 300mW SOD323	BZX384-C36,115	Nexperia

7 Transformer Specification (T1)

7.1 *Electrical Diagram*

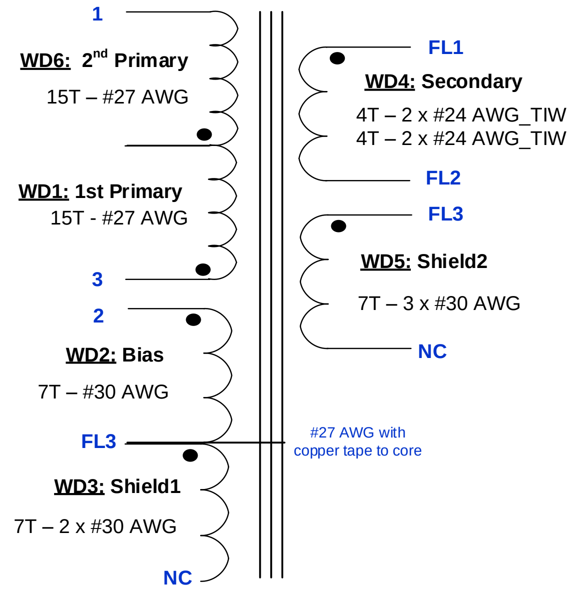

Figure 10 – Transformer Electrical Diagram.

7.2 *Electrical Specifications*

Parameter	Condition	Spec.
Nominal Primary Inductance	Across Pin 1 to Pin 3, with all other windings open LCR meter L_S measurement, 100 kHz, 1.0 V test level	425 uH ± 7%
Primary Leakage Inductance	Across Pin 1 to Pin 3, with FL1 and FL2 shorted LCR meter L_S measurement, 100 kHz, 1.0 V test level	5.5 uH (max)
Resonant Frequency	Across Pin 1 to Pin 3, with all other windings open	1,200 kHz (min)
Electrical Strength (Primary to Secondary)	Across shorted Primary windings (Pins 1, 2, 3, FL3) to shorted Secondary winding (FL1, FL2)	3000 VAC, 200 V/s ramp rate, 60 sec soak

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7.3 ***Transformer Build Diagram***

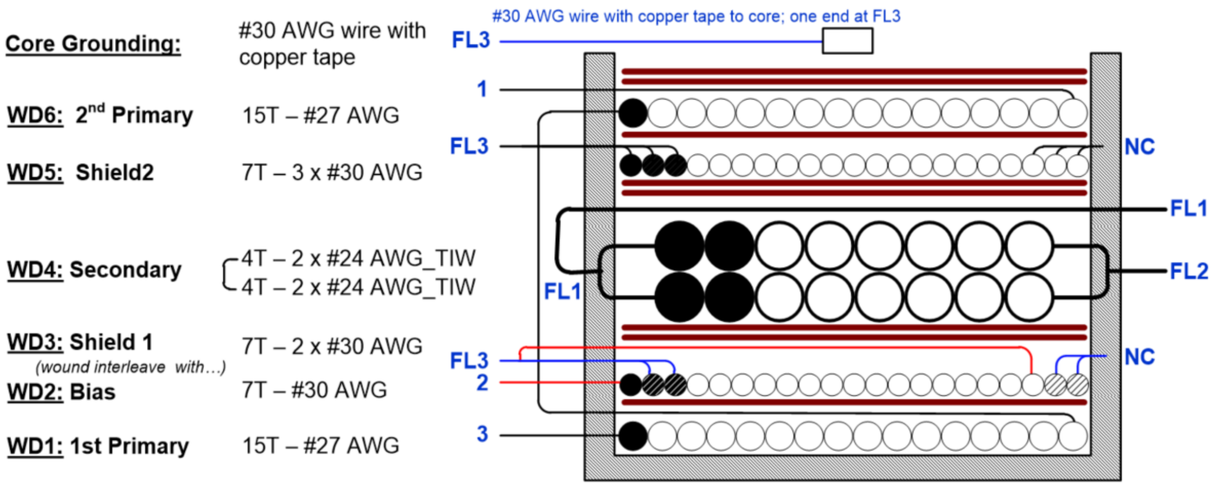

Figure 11 – Transformer Build Diagram.

7.4 ***Material List***

Item	Description
[1]	Core: ATQ23.7-14, Mg/Zn Ferrite material. PI#: 99-00072-00.
[2]	Bobbin: ATQ23.7-14 horizontal. PI#: 25-01171-00.
[3]	Magnet Wire: #27 AWG, Double Coated.
[4]	Magnet Wire: #30 AWG, Double Coated.
[5]	Magnet Wire: #24 AWG, Triple Insulated Wire.
[6]	Copper Foil: Copper Tape, 1 mil Thickness, 8.6 mm Width x 10.0 mm Length.
[7]	Tape: 3M 1350-F, Polyester Film, 1 mil Thickness, 7.0 mm Width.
[8]	Tape: 3M 1350-F, Polyester Film, 1 mil Thickness, 20 mm Width.
[9]	Tape: 3M 1350-F, Polyester Film, 1 mil Thickness, 12.4 mm Width.
[10]	Tape: 3M 1350-F, Polyester Film, 1 mil Thickness, 18.2 mm Width.
[11]	Tape: 3M 1350-F, Polyester Film, 1 mil Thickness, 5.6 mm Width.
[12]	Heat shrink: Heat shrink 3/32" inner diameter, Alpha Wire F221B3/32 BK100 or equivalent, cut into ~34 mm length
[13]	Varnish: Dolph BC-359.

7.5 *Bobbin Preparation*

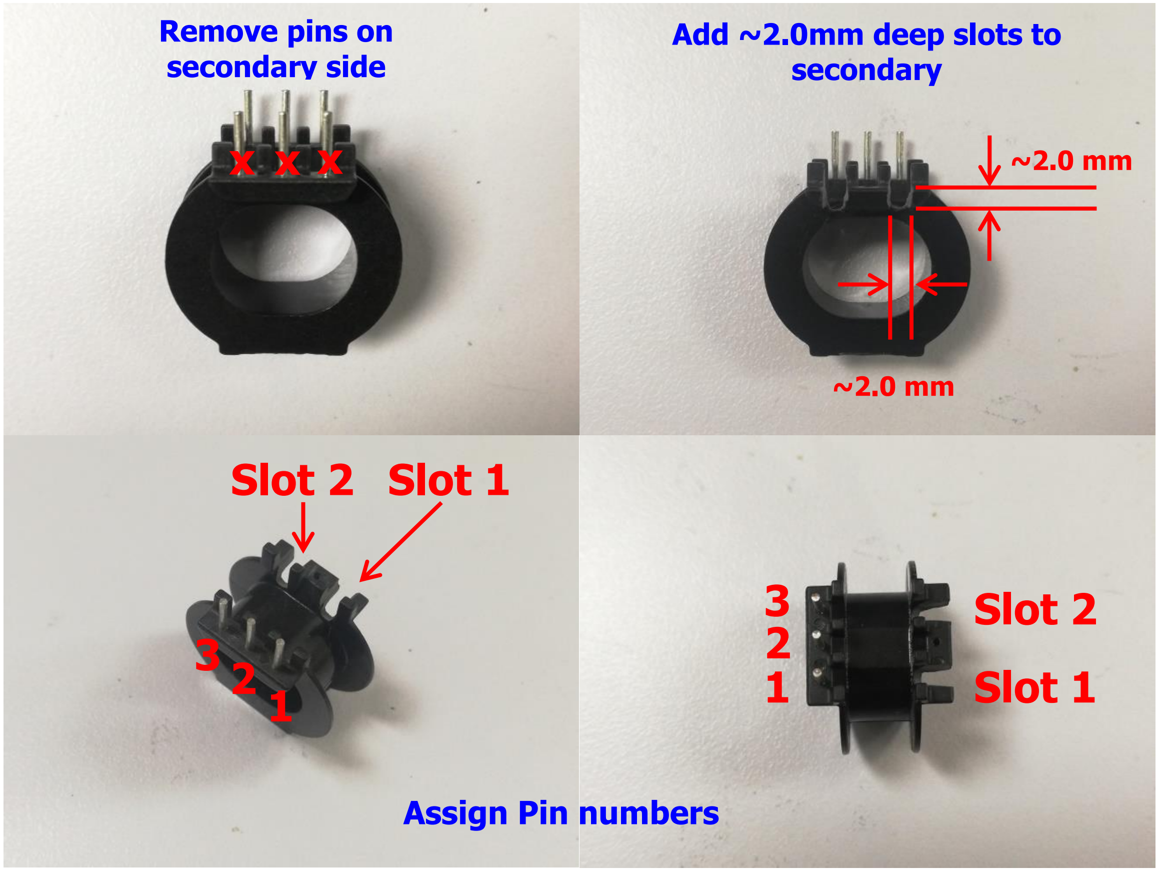

Figure 12 – Transformer Bobbin Modification and Pin Assignment.

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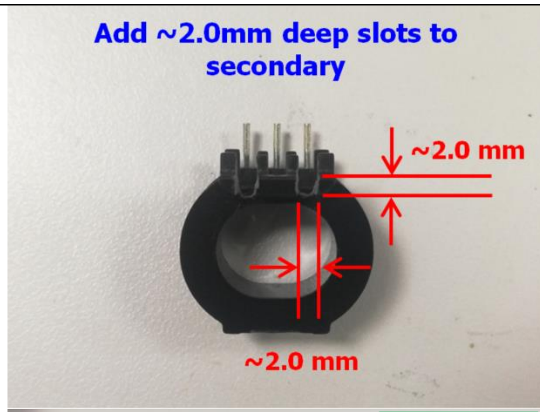
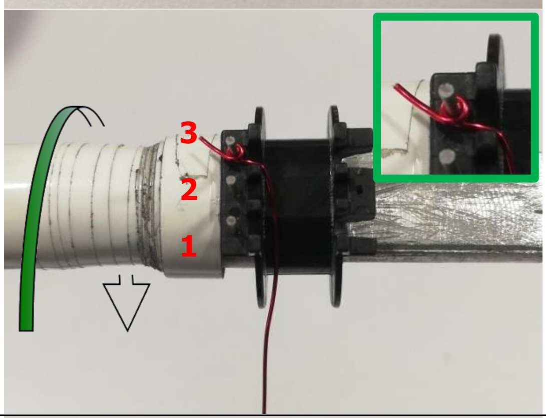
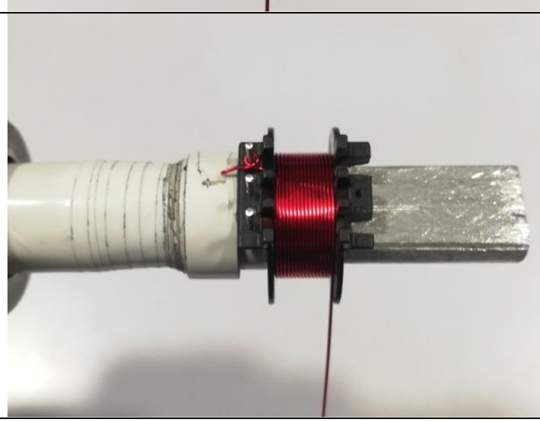
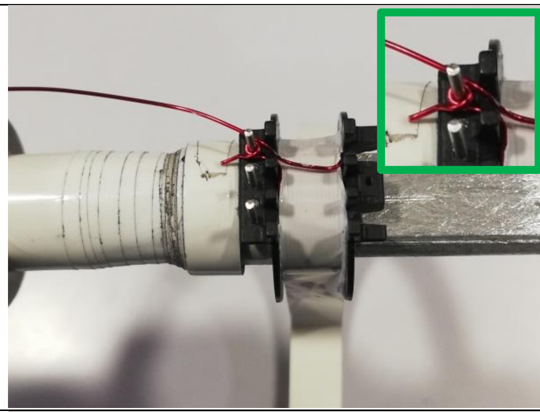
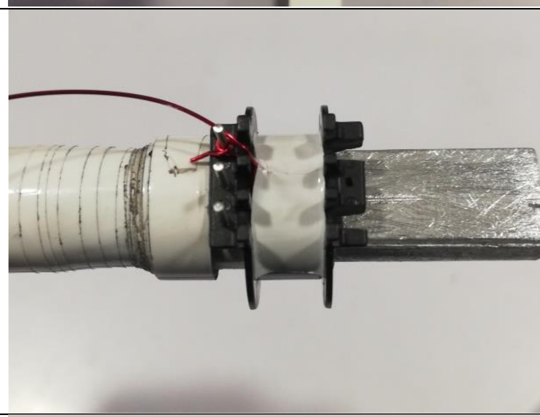
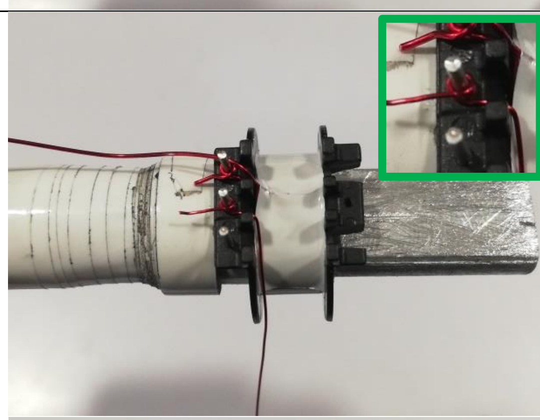
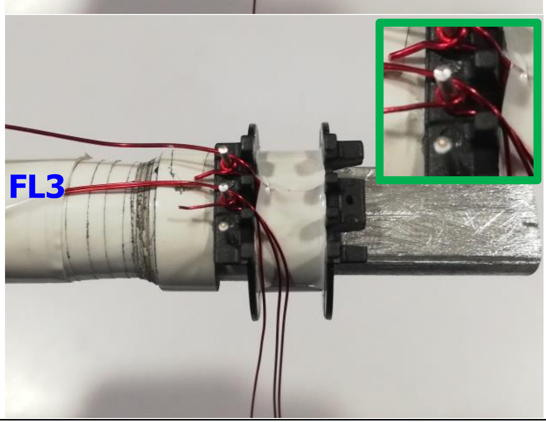
7.6 *Winding Instructions*

Bobbin and Winding Preparation	 	Remove pins on the secondary side and use a file or any appropriate grinding tool to create two ~2mm deep slots as illustrated in Bobbin Preparation section above. Position the bobbin on the mandrel such that the pin side of the bobbin is on the left side. Rotation of the mandrel is clock-wise as seen from the right side of the setup.
WD1 **1st Primary**		Start at pin 3, wind 15 turns of wire Item [3] in 1 layer, from left to right.

		At the end of last turn, place tape Item [7] to secure the winding, then bring back wire to the left side. Leave enough wire for the 2nd half Primary (15 turns) to be wound later.
Insulation		1 layer of tape Item [7].
WD2: Bias **&** **WD3: Shield 1**		Start at pin 2, with 1 wire Item [4] for WD2 (Bias).
		Start another 2 wires Item [4] for WD3 (Shield), leave ~2" floating and mark as FL3.

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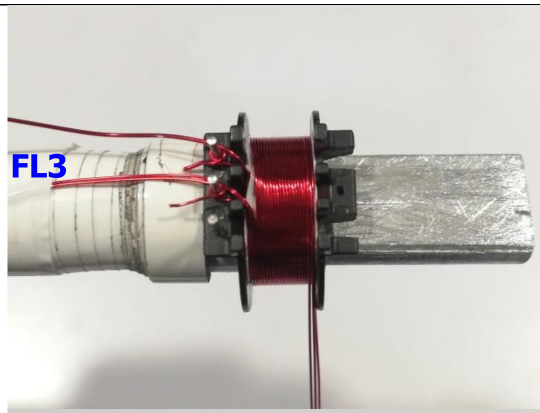
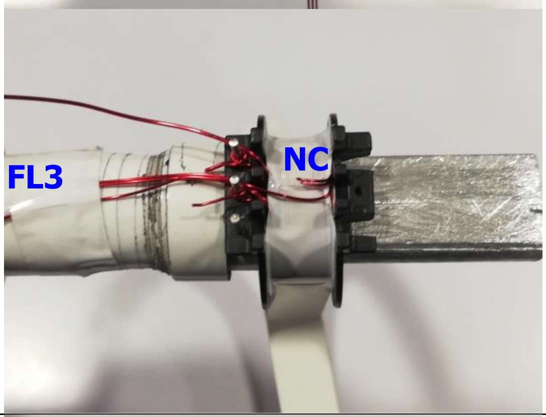
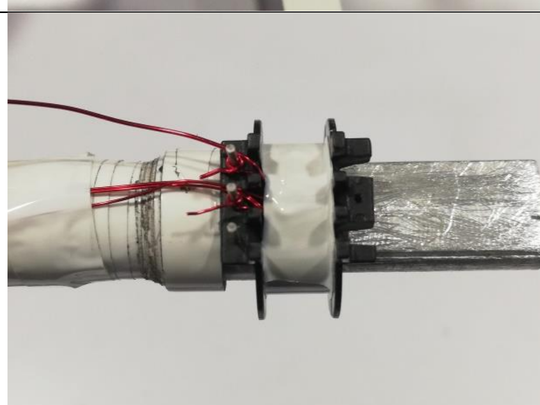
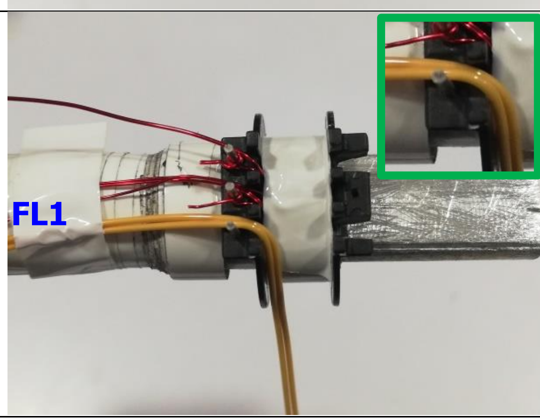
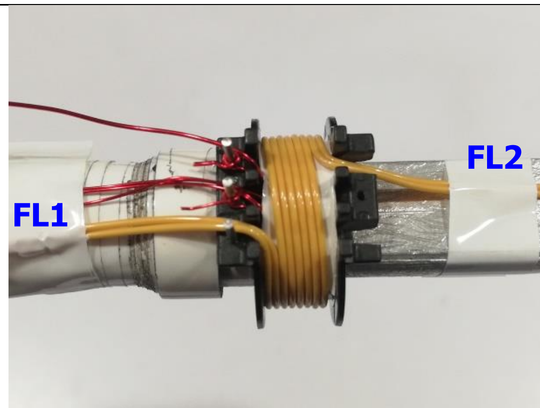
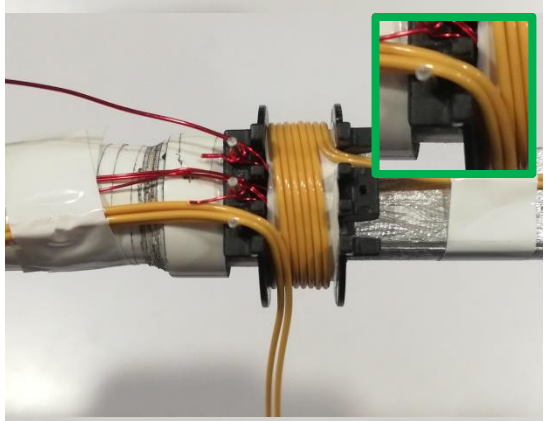
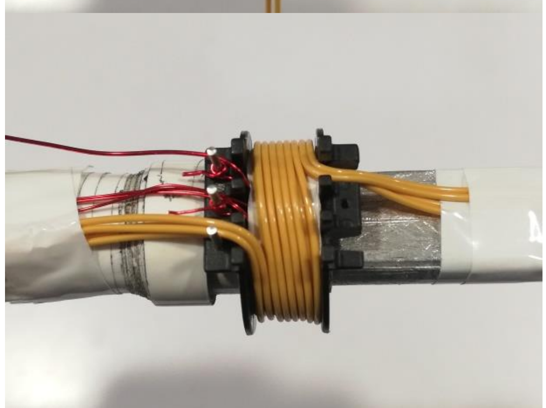
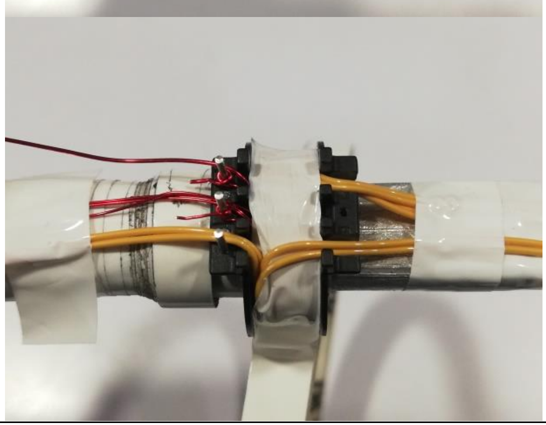
		Wind all 3 wires 7 turns in parallel.
		At the end of last turn, place tape Item [7] to secure the winding, then bring back 1 wire of WD2 to the left side and combine with FL3, and cut short 2 wires for WD3 as No-Connect.
Insulation		2 layers of tape Item [7].
WD4 Secondary		Temporarily start at the slot of Pin 1. Use 2 wires Item [5], leave ~2” floating, and mark as FL1.

		Wind 4 turns in 1 layer. At the end of last turn, exit the wires at the Slot 2, leave ~2" floating and mark as FL2 for 1st half of Secondary.
		Repeat another winding same as above for 2nd half of Secondary, which is parallel with 1st half Secondary.
		
		At the end of last turn, place tape Item [7] to secure the winding, then bring all 4 wires of FL1 to the right into Slot 1.

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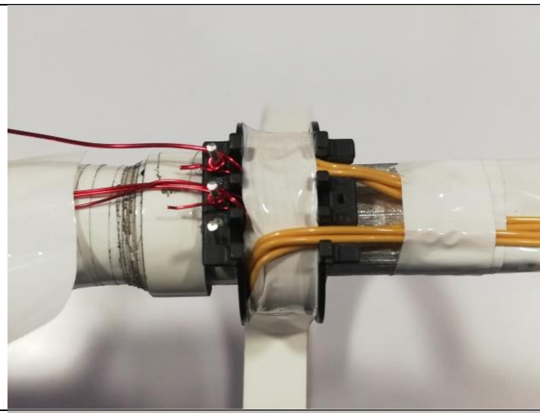
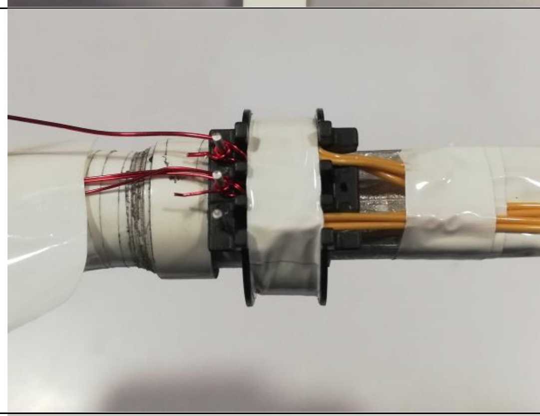
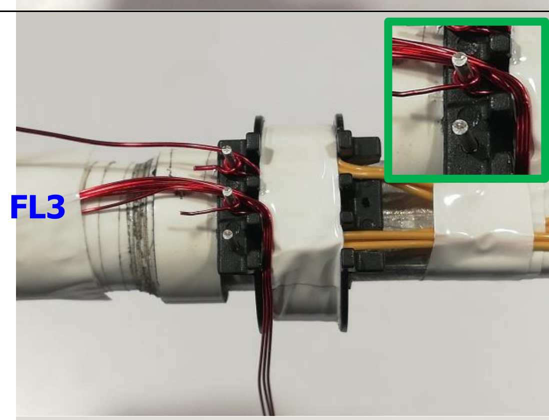
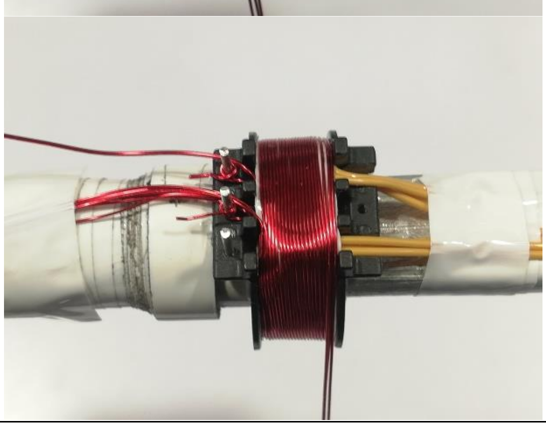
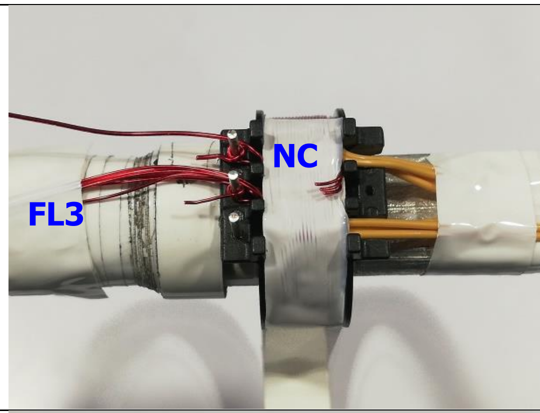
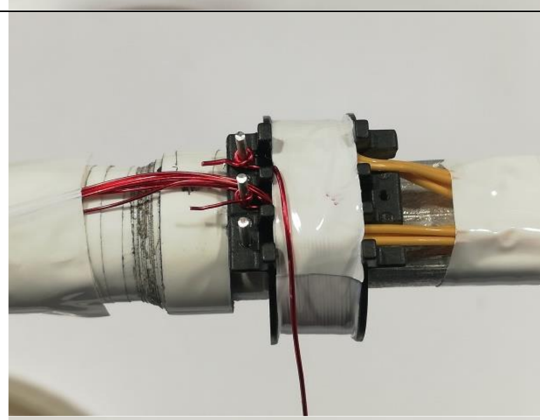
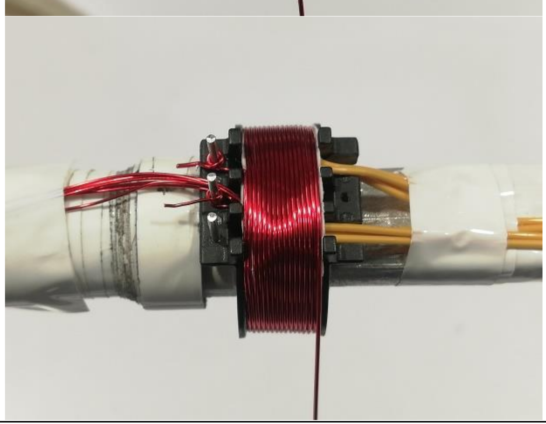
		
Insulation		2 layers of tape Item [7].
WD5 **Shield2**	 	Start at FL3, use 3 wires Item [4] and wind 7 turns in parallel.

		At the end of last turn, place tape Item [7] to secure the winding, then cut short the wires as No-Connect.
Insulation		1 layer of tape Item [7].
WD6 **2nd Primary**	 	Use wire hanging from WD1 and continue winding 15 turns from left to right.

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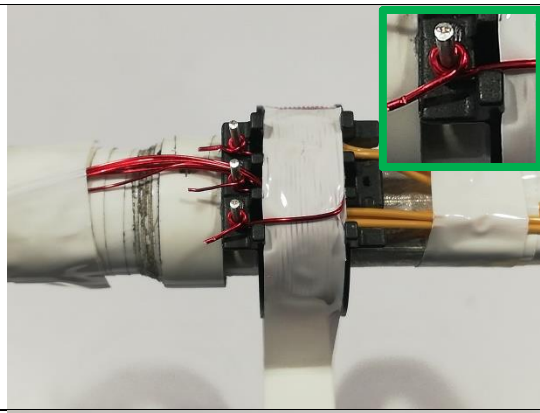
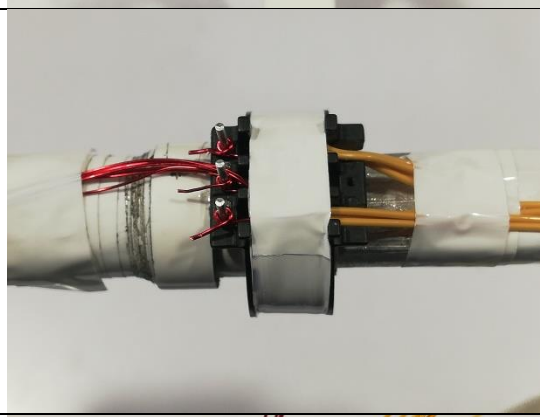
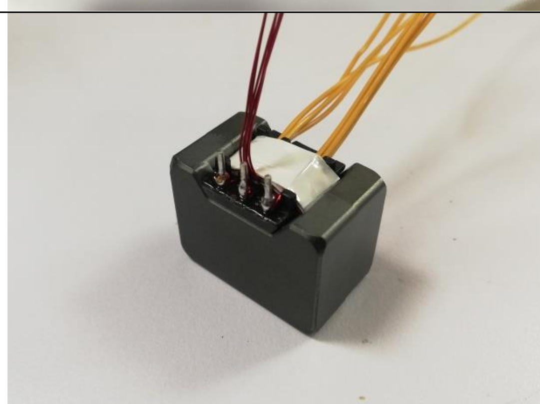
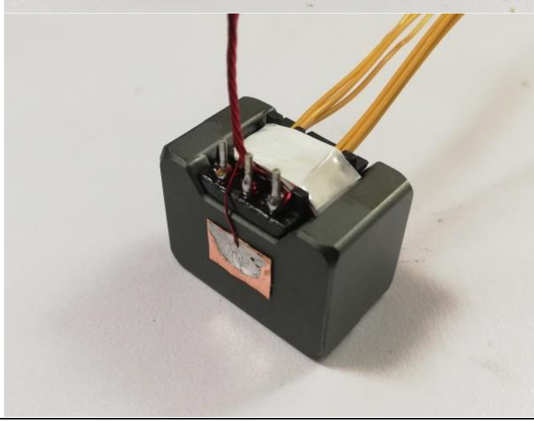
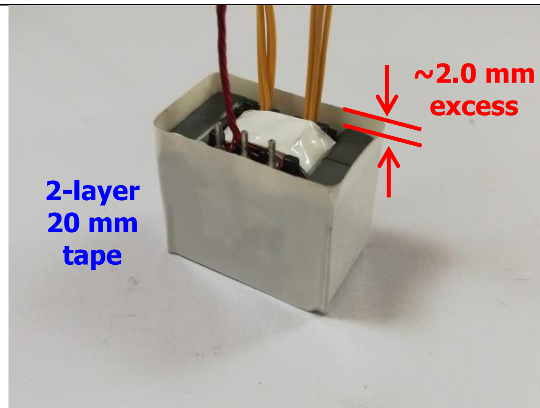
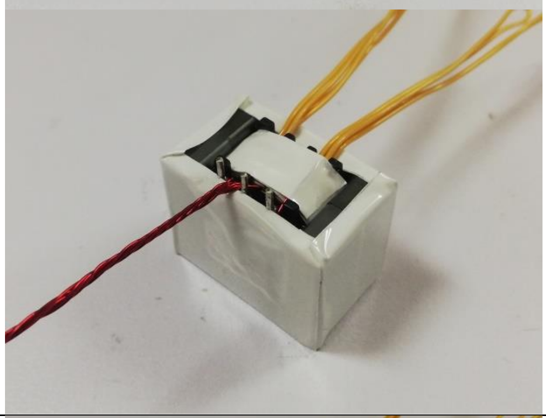
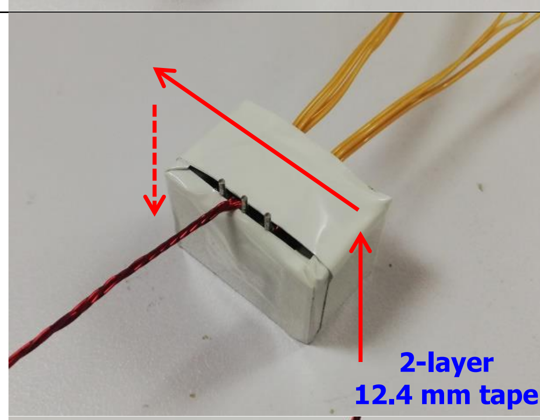
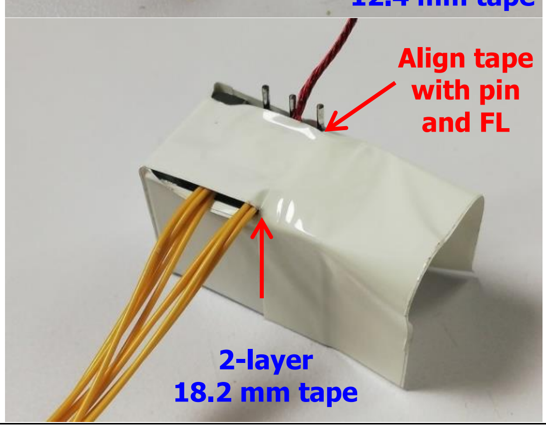
		At the end of last turn, place tape Item [7] to secure the winding, then finish winding at Pin 1.
Insulation		2 layers of tape Item [7].
Gap and Ground Core	 	Add gap to the middle leg of core Item [1] to get 425 μH ±7% primary inductance. Solder one end of wire Item [4] to copper tape Item [6]. Combine the wire with FL3, and attach the copper tape to the transformer core side.

		Secure core halves by wrapping 2 layers of tape Item [8] along the transformer sides. Align the tape such that ~2mm tape is extending on transformer bottom. Ensure primary inductance is still 425 µH ±7%.
		Fold the excess tape into the transformer bottom.
Tape for Core Insulation		Cover the transformer core bottom with 2 layers of tape Item [9] for improved ESD performance.
		Also secure the corners where the core is exposed with 2 layers of tape Item [10]. Align the edge of the tape to the primary pin and secondary wire.

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<table>
<tr>
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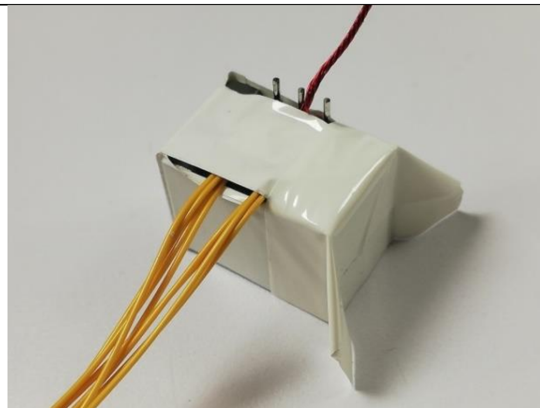
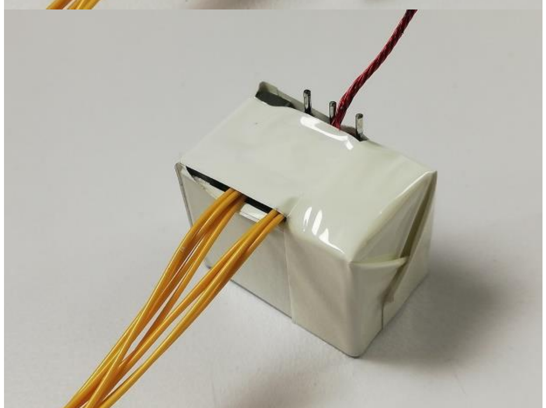
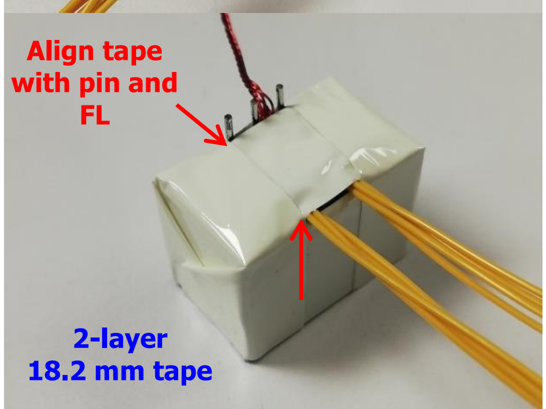
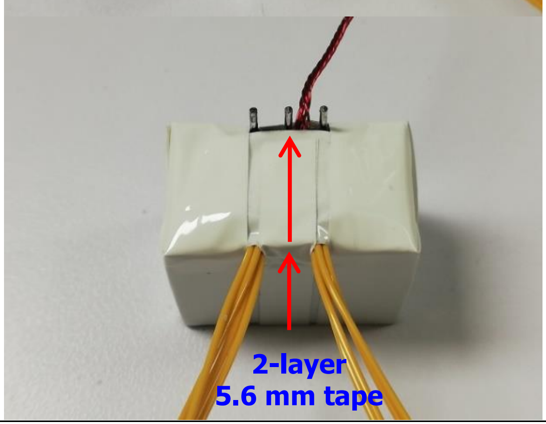
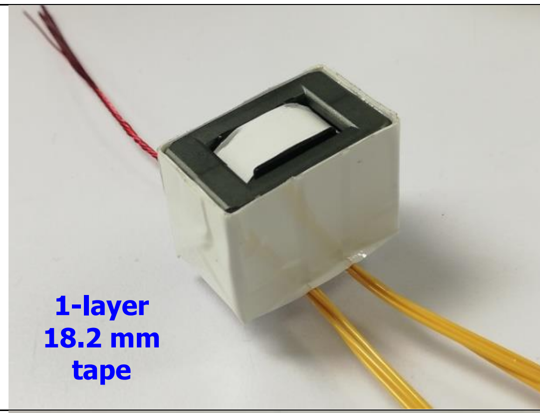
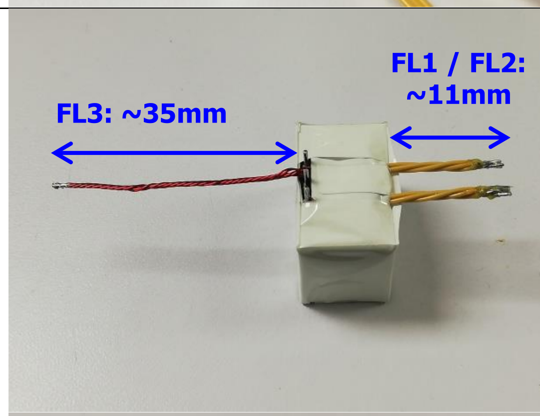
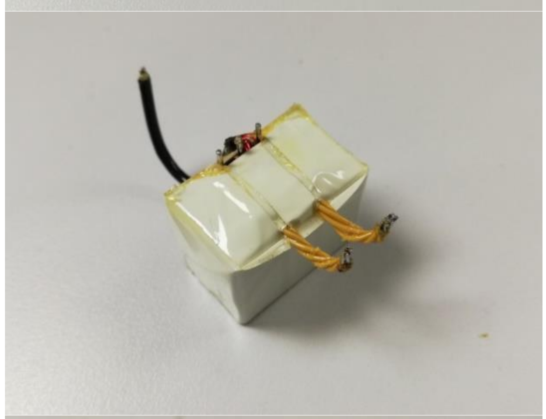
<td>






</td>
<td>Also cover the opening between FL1 and FL2 with 2 layers of tape Item [11].</td>
</tr>
</table>

		Wrap around the core sides with 1 layer tape Item [10] to secure the assembly.
Finish Assembly		Cut FL3 to ~35mm length and FL1 / FL2 to ~11mm length.
		Wrap FL3 with heat shrink Item [12].
		Varnish the transformer with Item [13].

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8 Common Mode Choke Specifications

8.1 *750 µH Common Mode Choke (L1)*

8.1.1 Electrical Diagram

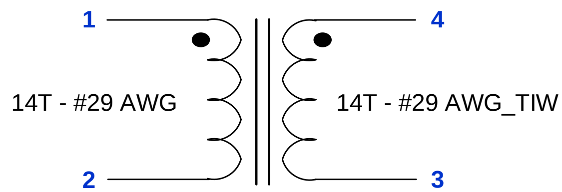


Figure 13 – Inductor Electrical Diagram.

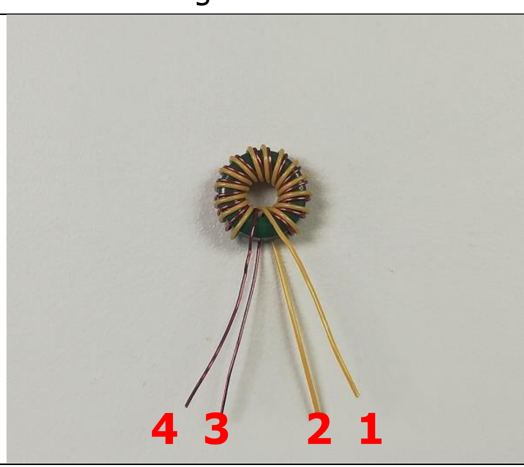
8.1.2 Electrical Specifications

Inductance	Across Pin 1 to Pin 2 (or Pin 4 to Pin 3) with the other winding open.	750 µH ±10%
Leakage Inductance	Across Pin 1 to Pin 2 (or Pin 4 to Pin 3) with the other winding shorted.	0.3 µH (Max.)
LCR Meter Setting	L_S measurement, 100 kHz switching frequency, 1.0 V test level.	

8.1.3 Material List

Item	Description
[1]	Core, Ferrite Inductor Toroid, 9 mm OD x 5 mm ID x 3 mm H PI#: 32-00330-00.
[2]	Magnet Wire: #29 AWG, Triple Insulated Wire.
[3]	Magnet Wire: #29 AWG, Double Coated.
[4]	Varnish: Dolph BC-359.

8.1.4 Winding Instructions



Start as Pin 1 for Item [2] and Pin 4 for Item [3].

Wind together 14 turns to core Item [1].

Mark end of Item [2] as Pin 2 and end of Item [3] as Pin 3.

Varnish the CMC using Item [4].

8.2 ***19.8 mH Common Mode Choke (L2)***

8.2.1 Electrical Diagram

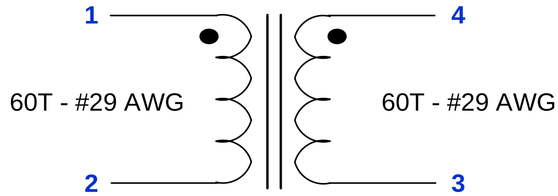


Figure 14 – Inductor Electrical Diagram.

8.2.2 Electrical Specifications

Inductance	Across Pin 1 to Pin 2 (or Pin 4 to Pin 3) with the other winding open.	19.8 mH ±25%
Leakage Inductance	Across Pin 1 to Pin 2 (or Pin 4 to Pin 3) with the other winding shorted.	100 μH (Max.)
LCR Meter Setting	L_S measurement, 100 kHz switching frequency, 1.0 V test level	

8.2.3 Material List

Item	Description
[1]	Core, Ferrite Inductor Toroid, 14.90 mm OD x 6.5 mm Th x 7.0 mm ID. PI#: 32-00286-00.
[2]	Cable Tie, PLT.6SM-M, 1.8mm Thick. PI#: 75-00202-00
[3]	Magnet Wire: #29 AWG, Double Coated.
[4]	Varnish: Dolph BC-359.
[5]	Heat shrink: Heat shrink 1” Inner diameter, 0.035” Wall Thickness. PI#: 62-00002-00; cut to 0.75” length

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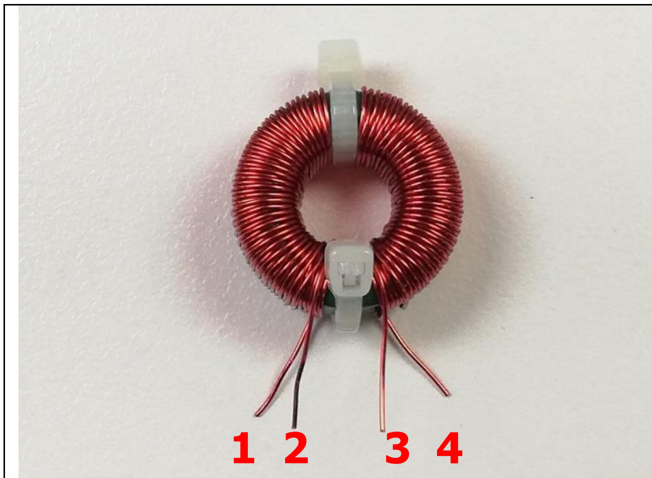
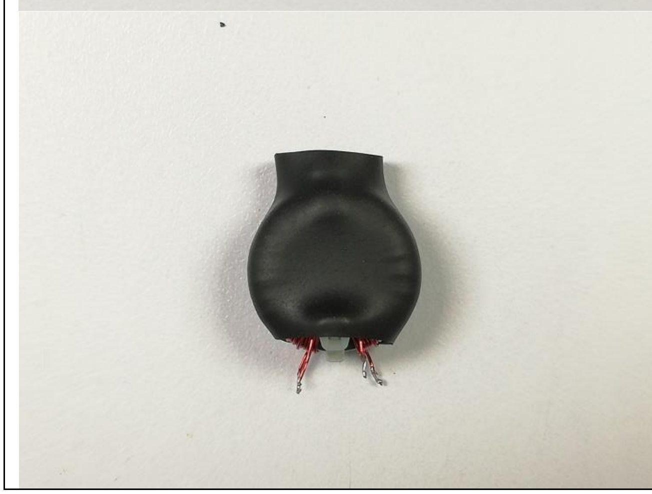
8.2.4 Winding Instructions





Place cable ties Item [2] to divide core Item [1] into two sections.

Start as Pin 1 with Item [3], wind 60 turns in two layers (32 turn on first layer + 28 turns on 2nd layer) on the one core half. Mark end of wire as Pin 2.

Repeat 60 turns of Item [3] on the next core half, starting as Pin 4 and end as Pin 3.

Varnish the CMC using Item [4].

Cover with heat shrink tube Item [5].

9 Transformer Design Spreadsheet

1	ACDC_InnoSwitch3-Pro_Flyback_050420; Rev.1.3; Copyright Power Integrations 2020	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-Pro Flyback Design Spreadsheet
2	APPLICATION VARIABLES					
3	VAC_MIN	90		90	V	Minimum AC line voltage
4	VAC_MAX	265		265	V	Maximum AC input voltage
5	VAC_RANGE			UNIVERSAL		AC line voltage range
6	FLINE			60	Hz	AC line voltage frequency
7	CAP_INPUT	45.0		45.0	uF	Input capacitance
9	SET-POINT 1					
10	VOUT1	21.00		21.00	V	Output voltage 1, should be the highest output voltage required
11	IOUT1	1.400		1.400	A	Output current 1
12	POUT1			29.40	W	Output power 1
13	EFFICIENCY1	0.91		0.91		Converter efficiency for output 1
14	Z_FACTOR1	0.50		0.50		Z-factor for output 1
16	SET-POINT 2					
17	VOUT2	20.00		20.00	V	Output voltage 2
18	IOUT2	1.500		1.500	A	Output current 2
19	POUT2			30.00	W	Output power 2
20	EFFICIENCY2	0.91		0.91		Converter efficiency for output 2
21	Z_FACTOR2	0.50		0.50		Z-factor for output 2
23	SET-POINT 3					
24	VOUT3	15.00		15.00	V	Output voltage 3
25	IOUT3	2.000		2.000	A	Output current 3
26	POUT3			30.00	W	Output power 3
27	EFFICIENCY3	0.91		0.91		Converter efficiency for output 3
28	Z_FACTOR3	0.50		0.50		Z-factor for output 3
30	SET-POINT 4					
31	VOUT4	11.00		11.00	V	Output voltage 4
32	IOUT4	2.700		2.700	A	Output current 4
33	POUT4			29.70	W	Output power 4
34	EFFICIENCY4	0.91		0.91		Converter efficiency for output 4
35	Z_FACTOR4	0.50		0.50		Z-factor for output 4
37	SET-POINT 5					
38	VOUT5	10.00		10.00	V	Output voltage 5
39	IOUT5	3.000		3.000	A	Output current 5
40	POUT5			30.00	W	Output power 5
41	EFFICIENCY5	0.91		0.91		Converter efficiency for output 5
42	Z_FACTOR5	0.50		0.50		Z-factor for output 5
44	SET-POINT 6					
45	VOUT6	9.00		9.00	V	Output voltage 6
46	IOUT6	3.000		3.000	A	Output current 6
47	POUT6			27.00	W	Output power 6
48	EFFICIENCY6	0.90		0.90		Converter efficiency for output 6
49	Z_FACTOR6	0.50		0.50		Z-factor for output 6
51	SET-POINT 7					
52	VOUT7	5.00		5.00	V	Output voltage 7
53	IOUT7	3.000		3.000	A	Output current 7
54	POUT7			15.00	W	Output power 7
55	EFFICIENCY7	0.90		0.90		Converter efficiency for output 7
56	Z_FACTOR7	0.50		0.50		Z-factor for output 7
58	SET-POINT 8					
59	VOUT8			0.00	V	Output voltage 8
60	IOUT8			0.000	A	Output current 8
61	POUT8			0.00	W	Output power 8
62	EFFICIENCY8			0.00		Converter efficiency for output 8
63	Z_FACTOR8			0.00		Z-factor for output 8

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65	**SET-POINT 9**					
66	VOUT9			0.00	V	Output voltage 9
67	IOUT9			0.000	A	Output current 9
68	POUT9			0.00	W	Output power 9
69	EFFICIENCY9			0.00		Converter efficiency for output 9
70	Z_FACTOR9			0.00		Z-factor for output 9
71						
72	VOLTAGE_CDC	0.000		0.000	V	Cable drop compensation desired at maximum output current
76	**PRIMARY CONTROLLER SELECTION**					
77	ENCLOSURE	ADAPTER		ADAPTER		Power supply enclosure
78	ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
79	VDRAIN_BREAKDOWN	750		750	V	Device breakdown voltage
80	DEVICE_GENERIC	INN33X8		INN33X8		Device selection
81	DEVICE_CODE			INN3378C		Device code
82	PDEVICE_MAX			55	W	Device maximum power capability
83	RDSON_25DEG			0.68	Ω	Primary switch on-time resistance at 25°C
84	RDSON_100DEG			1.02	Ω	Primary switch on-time resistance at 100°C
85	ILIMIT_MIN			1.767	A	Primary switch minimum current limit
86	ILIMIT_TYP			1.900	A	Primary switch typical current limit
87	ILIMIT_MAX			2.033	A	Primary switch maximum current limit
88	VDRAIN_ON_PRSW			0.38	V	Primary switch on-time voltage drop
89	VDRAIN_OFF_PRSW			600.71	V	Peak drain voltage on the primary switch during turn-off
93	**WORST CASE ELECTRICAL PARAMETERS**					
94	FSWITCHING_MAX	58635		58635	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
95	VOR	157.4		157.4	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
96	VMIN			85.33	V	Valley of the rectified minimum input AC voltage at full load
97	KP			1.048		Measure of continuous/discontinuous mode of operation
98	MODE_OPERATION			DCM		Mode of operation
99	DUTYCYCLE			0.458		Primary switch duty cycle
100	TIME_ON			9.54	us	Primary switch on-time
101	TIME_OFF			9.39	us	Primary switch off-time
102	LPRIMARY_MIN			395.3	uH	Minimum primary magnetizing inductance
103	LPRIMARY_TYP			425.0	uH	Typical primary magnetizing inductance
104	LPRIMARY_TOL	7.0		7.0	%	Primary magnetizing inductance tolerance
105	LPRIMARY_MAX			454.8	uH	Maximum primary magnetizing inductance
107	**PRIMARY CURRENT**					
108	IAVG_PRIMARY			0.371	A	Primary switch average current
109	IPEAK_PRIMARY			1.823	A	Primary switch peak current
110	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
111	IRIPPLE_PRIMARY			1.823	A	Primary switch ripple current
112	IRMS_PRIMARY			0.671	A	Primary switch RMS current
114	**SECONDARY CURRENT**					
115	IPEAK_SECONDARY			13.670	A	Secondary winding peak current
116	IPEDESTAL_SECONDARY			0.000	A	Secondary winding pedestal current
117	IRMS_SECONDARY			5.344	A	Secondary winding RMS current

118	IRIPPLE_CAP_OUT			4.423	A	Output capacitor ripple current
122	**TRANSFORMER CONSTRUCTION PARAMETERS**					
123	**CORE SELECTION**					
124	CORE	CUSTOM	Info	CUSTOM		The transformer windings may not fit: pick a bigger core or bobbin and refer to the Transformer Parameters tab for fit calculations
125	CORE NAME	ATQ23.7-14		ATQ23.7-14		Core code
126	AE	103.0		103.0	mm^2	Core cross sectional area
127	LE	38.2		38.2	mm	Core magnetic path length
128	AL	7200		7200	nH	Ungapped core effective inductance per turns squared
129	VE	3934		3934	mm^3	Core volume
130	BOBBIN NAME	BAQT23.7-14		BAQT23.7-14		Bobbin name
131	AW	24.4		24.4	mm^2	Bobbin window area
132	BW	6.60		6.60	mm	Bobbin width
133	MARGIN	0.0		0.0	mm	Bobbin safety margin
135	**PRIMARY WINDING**					
136	NPRIMARY			30		Primary winding number of turns
137	BPEAK			3062	Gauss	Peak flux density
138	BMAX			2623	Gauss	Maximum flux density
139	BAC			1311	Gauss	AC flux density (0.5 x Peak to Peak)
140	ALG			472	nH	Typical gapped core effective inductance per turns squared
141	LG			0.256	mm	Core gap length
142	LAYERS_PRIMARY	2		2		Primary winding number of layers
143	AWG_PRIMARY			27		Primary wire gauge
144	OD_PRIMARY_INSULATED			0.418	mm	Primary wire insulated outer diameter
145	OD_PRIMARY_BARE			0.361	mm	Primary wire bare outer diameter
146	CMA_PRIMARY			300.3	Cmils/A	Primary winding wire CMA
148	**SECONDARY WINDING**					
149	NSECONDARY	4		4		Secondary winding number of turns
150	AWG_SECONDARY			19		Secondary wire gauge
151	OD_SECONDARY_INSULATED			1.217	mm	Secondary wire insulated outer diameter
152	OD_SECONDARY_BARE			0.912	mm	Secondary wire bare outer diameter
153	CMA_SECONDARY			241.0	Cmils/A	Secondary winding wire CMA
155	**BIAS WINDING**					
156	NBIAS			6		Bias winding number of turns
160	**PRIMARY COMPONENTS SELECTION**					
161	**LINE UNDERVOLTAGE**					
162	BROWN-IN REQURED	76.00		76.00	V	Required line brown-in threshold
163	RLS			3.82	MΩ	Connect two 1.91 MOhm resistors to the V-pin for the required UV/OV threshold
164	BROWN-IN ACTUAL			76.58	V	Actual brown-in threshold using standard resistors
165	BROWN-OUT ACTUAL			69.26	V	Actual brown-out threshold using standard resistors
167	**LINE OVERVOLTAGE**					
168	OVERVOLTAGE_LINE		Warning	319.20	V	The device voltage stress will be higher than 650V when overvoltage is trigerred
170	**BIAS WINDING**					
171	VBIAS	6.10	Info	6.10	V	The rectified bias voltage maybe too low to supply the BP pin: Increase the rectified bias voltage to a value higher than 9V
172	VF_BIAS			0.70	V	Bias winding diode forward drop
173	VREVERSE_BIASDIODE			80.76	V	Bias diode reverse voltage (not

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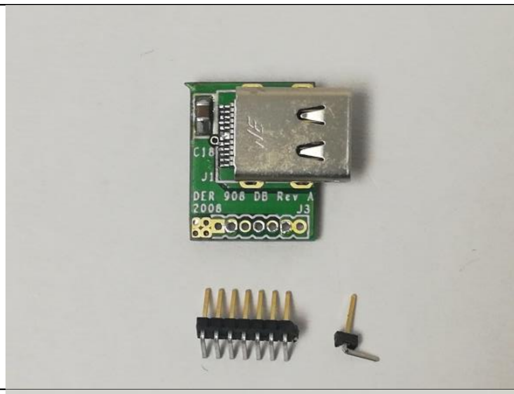
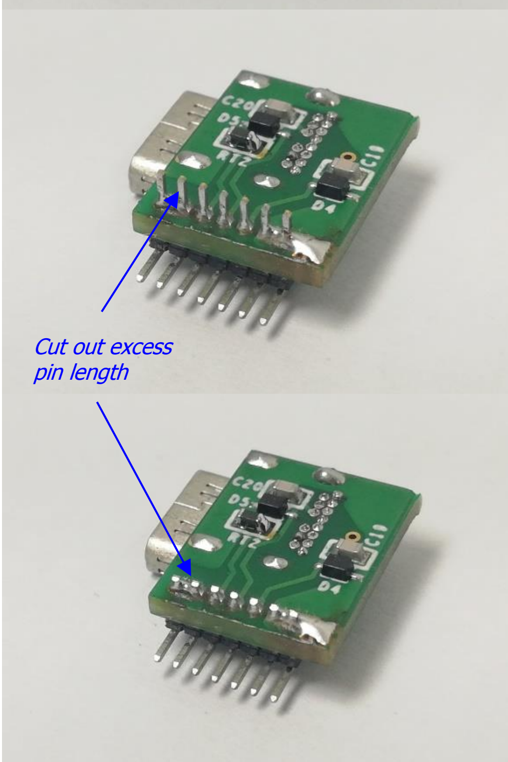
						accounting parasitic voltage ring)
174	CBIAS			22	uF	Bias winding rectification capacitor
175	CBPP			4.70	uF	BPP pin capacitor
179	**SECONDARY COMPONENTS SELECTION**					
180	**RECTIFIER**					
181	VDRAIN_OFF_SRFET			70.77	V	Secondary rectifier reverse voltage (not accounting parasitic voltage ring)
182	SRFET	AONS62922		AONS62922		Secondary rectifier (Logic MOSFET)
183	VBREAKDOWN_SRFET			120	V	Secondary rectifier breakdown voltage
184	RDSON_SRFET			7.0	mΩ	SRFET on time drain resistance at 25degC for VGS=4.4V
188	**SET-POINTS ANALYSIS**					
189	**TOLERANCE CORNER**					
190	USER_VAC	90		90	V	Input AC RMS voltage corner to be evaluated
191	USER_ILIMIT	MIN		1.767	A	Current limit corner to be evaluated
192	USER_LPRIMARY	MIN		395.3	uH	Primary inductance corner to be evaluated
194	**SET-POINT SELECTION**					
195	SET-POINT	2		2		Select the set-point which needs to be evaluated
196	FSWITCHING			58634.6	Hz	Switching frequency at full load and valley of the rectified minimum AC input voltage
197	VOR			149.9	V	Voltage reflected to the primary winding when the primary switch turns off
198	VMIN			85.33	V	Valley of the minimum input AC voltage
199	KP			2.160		Measure of continuous/discontinuous mode of operation
200	MODE_OPERATION			DCM		Mode of operation
201	DUTYCYCLE			0.450		Primary switch duty cycle
202	TIME_ON			7.67	us	Primary switch on-time
203	TIME_OFF			9.39	us	Primary switch off-time
205	**PRIMARY CURRENT**					
206	IAVG_PRIMARY			0.371	A	Primary switch average current
207	IPEAK_PRIMARY			1.648	A	Primary switch peak current
208	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
209	IRIPPLE_PRIMARY			1.648	A	Primary switch ripple current
210	IRMS_PRIMARY			0.638	A	Primary switch RMS current
212	**SECONDARY CURRENT**					
213	IPEAK_SECONDARY			12.362	A	Secondary winding peak current
214	IPEDESTAL_SECONDARY			0.000	A	Secondary winding pedestal current
215	IRMS_SECONDARY			3.603	A	Secondary winding RMS current
216	IRIPPLE_CAP_OUT			3.276	A	Output capacitor ripple current
218	**MAGNETIC FLUX DENSITY**					
219	BPEAK			2313	Gauss	Peak flux density
220	BMAX			2108	Gauss	Maximum flux density
221	BAC			1054	Gauss	AC flux density (0.5 x Peak to Peak)

10 Assembly Details

10.1 *USB Type-C PCB Assembly*

	Remove one pin from header J3 to reduce total pin count to 7.
 	Populate J3 to the USB Type-C PCB. Cut out excess pin length on the bottom side of the board.

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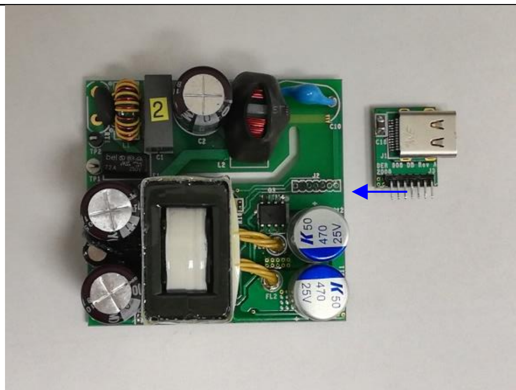 	Solder USB Type-C PCB header into the main board J2.
 	Verify that CMC L2 has heat shrink cover to prevent ESD arcing from USB Type-C PCB into the CMC winding.

11 Performance Data

Note: 1. Output voltage measured on the PCB unless otherwise specified.
2. Measurements taken at room temperature ambient (approximately 25 °C) unless otherwise specified.

11.1 *No-Load Input Power at 5 V_{OUT}*

Note: 1. Unit tested without Type-C cable connected to output.
2. For each line voltage, soak time = 10 min and integration time = 5 min.

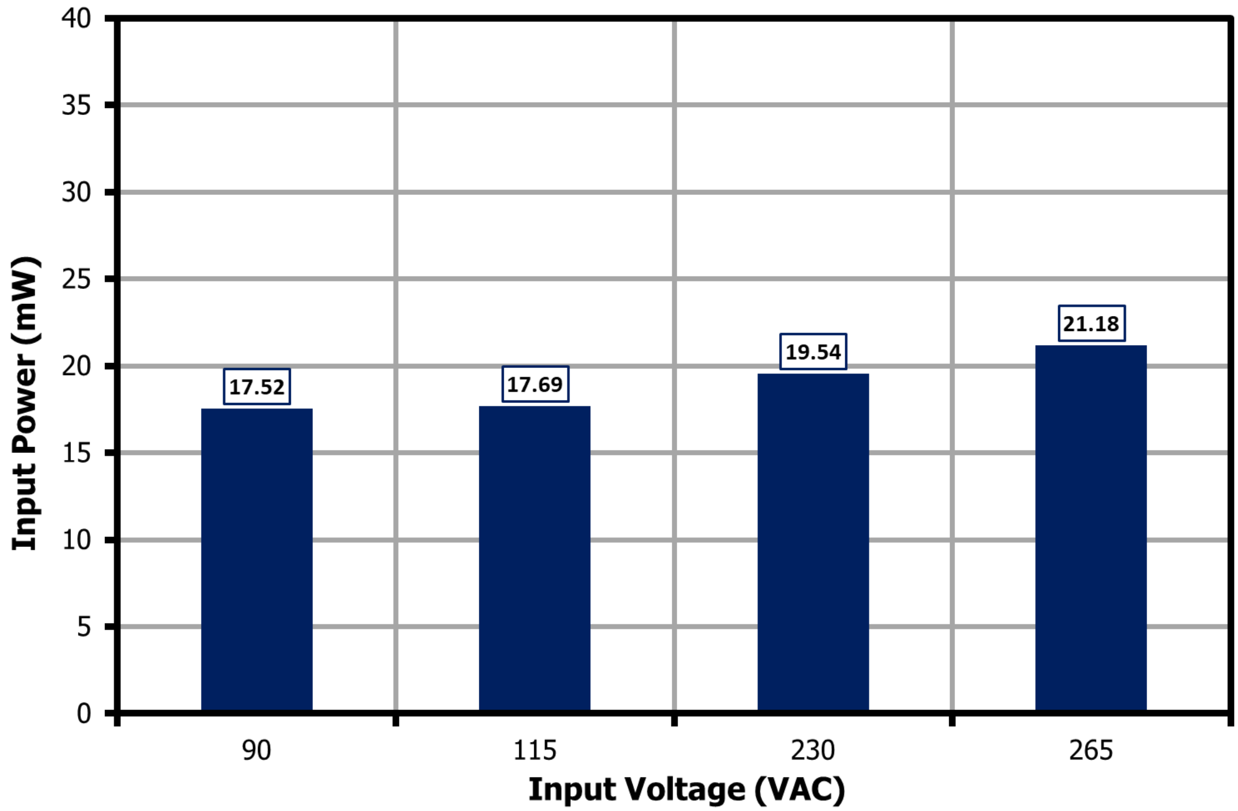

Figure 15 – No-Load Input Power vs. Input Line Voltage.

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11.2 *Full Load Efficiency*

V_{OUT} (V)	Load (A)	Power (W)	Full Load Efficiency (%)			
			90 VAC	115 VAC	230 VAC	265 VAC
5	3.0	15	89.74	90.42	90.23	89.77
9	3.0	27	90.38	91.46	92.04	91.72
15	2.0	30	90.92	92.06	92.76	92.52
20	1.5	30	90.85	91.98	92.65	92.41

11.3 *Average and 10% Load Efficiency*

11.3.1 Efficiency Requirements

		Test	Average	Average	10% Load
		Effective	2016	Jan-16	Jan-16
V_{OUT} (V)	Model (V)	Power (W)	New EISA2007	CoC v5 Tier 2	CoC v5 Tier 2
5	<6	15	81.39%	81.84%	72.48%
9	>6	27	86.62%	87.30%	77.30%
15	>6	30	86.95%	87.70%	77.70%
20	>6	30	86.95%	87.70%	77.70%

11.3.2 Efficiency Performance Summary (On Board)

V_{OUT} (V)	Power (W)	Average Efficiency (%)		10% Load Efficiency (%)	
		115 VAC	230 VAC	115 VAC	230 VAC
5	15	91.00	89.62	89.53	84.49
9	27	91.93	91.51	89.32	85.63
15	30	91.95	91.73	85.90	82.97
20	30	91.22	90.99	82.51	79.46

11.3.3 Average and 10% Load Efficiency Measurements

11.3.3.1 Output: 5 V / 3 A

Input (VAC)	Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)	DOE6 Requirement (%)	CoC v5 Tier 2 Requirement (%)	Remarks
115	100	14.97	90.50	**91.00**	81.39	81.84	PASS
	75	11.28	91.00				
	50	7.55	91.25				
	25	3.78	91.24				
	10	1.52	**89.53**			72.48	PASS
230	100	15.00	90.26	**89.62**	81.39	81.84	PASS
	75	11.29	90.34				
	50	7.56	89.85				
	25	3.78	88.04				
	10	1.52	**84.49**			72.48	PASS

11.3.3.2 Output: 9 V / 3 A

Input (VAC)	Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)	DOE6 Requirement (%)	CoC v5 Tier 2 Requirement (%)	Remarks
115	100	26.93	91.65	**91.93**	86.62	87.30	PASS
	75	20.26	91.97				
	50	13.54	92.23				
	25	6.78	91.87				
	10	2.71	**89.32**			77.30	PASS
230	100	26.96	92.05	**91.51**	86.62	87.30	PASS
	75	20.28	92.05				
	50	13.55	91.78				
	25	6.78	90.17				
	10	2.71	**85.63**			77.30	PASS

11.3.3.3 Output: 15 V / 2 A

Input (VAC)	Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)	DOE6 Requirement (%)	CoC v5 Tier 2 Requirement (%)	Remarks
115	100	30.01	92.25	**91.95**	86.95	87.70	PASS
	75	22.53	92.33				
	50	15.03	92.26				
	25	7.52	90.94				
	10	3.01	**85.90**			77.70	PASS
230	100	30.02	92.81	**91.73**	86.95	87.70	PASS
	75	22.54	92.59				
	50	15.04	91.96				
	25	7.52	89.55				
	10	3.01	**82.97**			77.70	PASS

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11.3.3.4 Output: 20 V / 1.5 A

Input (VAC)	Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)	DOE6 Requirement (%)	CoC v5 Tier 2 Requirement (%)	Remarks
115	100	29.98	92.14	**91.22**	86.95	87.70	PASS
	75	22.50	92.05				
	50	15.00	91.54				
	25	7.50	89.16				
	10	3.00	**82.51**			77.70	PASS
230	100	29.99	92.70	**90.99**	86.95	87.70	PASS
	75	22.50	92.28				
	50	15.01	91.18				
	25	7.50	87.81				
	10	3.00	**79.46**			77.70	PASS

11.4 *Efficiency Across Line at 100% Load (On Board)*

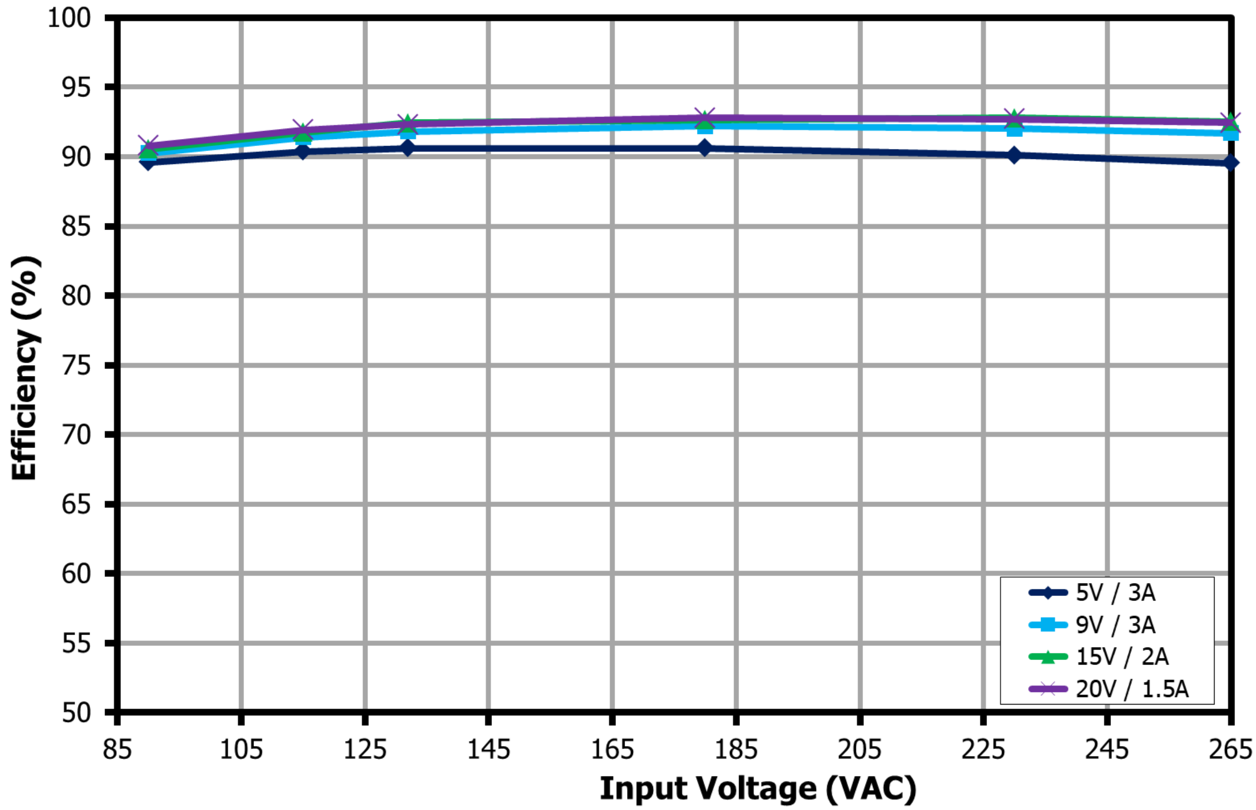

Figure 16 – Full Load Efficiency vs. Input Line for 5 V, 9 V, 15 V, and 20 V Output, Room Temperature.

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11.5 *Efficiency Across Load (On Board)*

11.5.1 Output: 5 V / 3 A

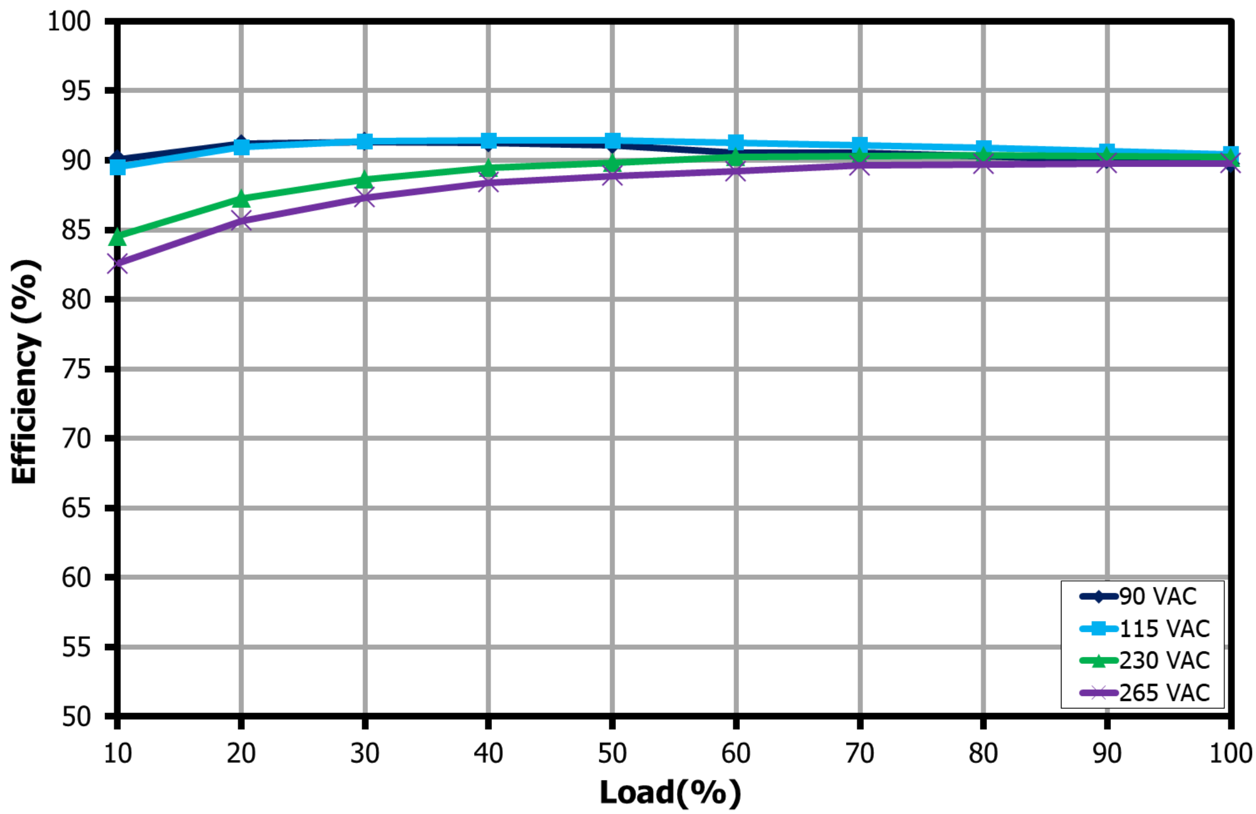

Figure 17 – Efficiency vs. Load for 5 V Output, Room Temperature.

11.5.2 Output: 9 V / 3 A

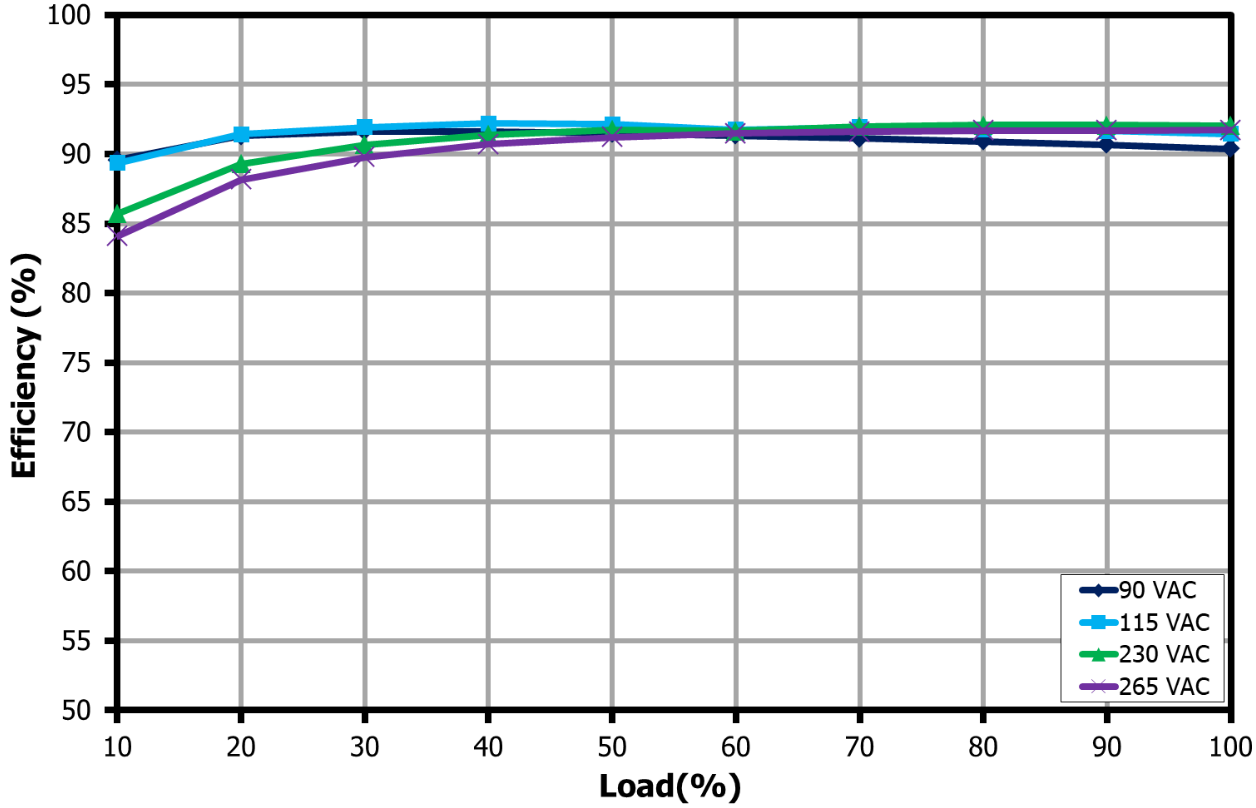

Figure 18 – Efficiency vs. Load for 9 V Output, Room Temperature.

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11.5.3 Output: 15 V / 2 A

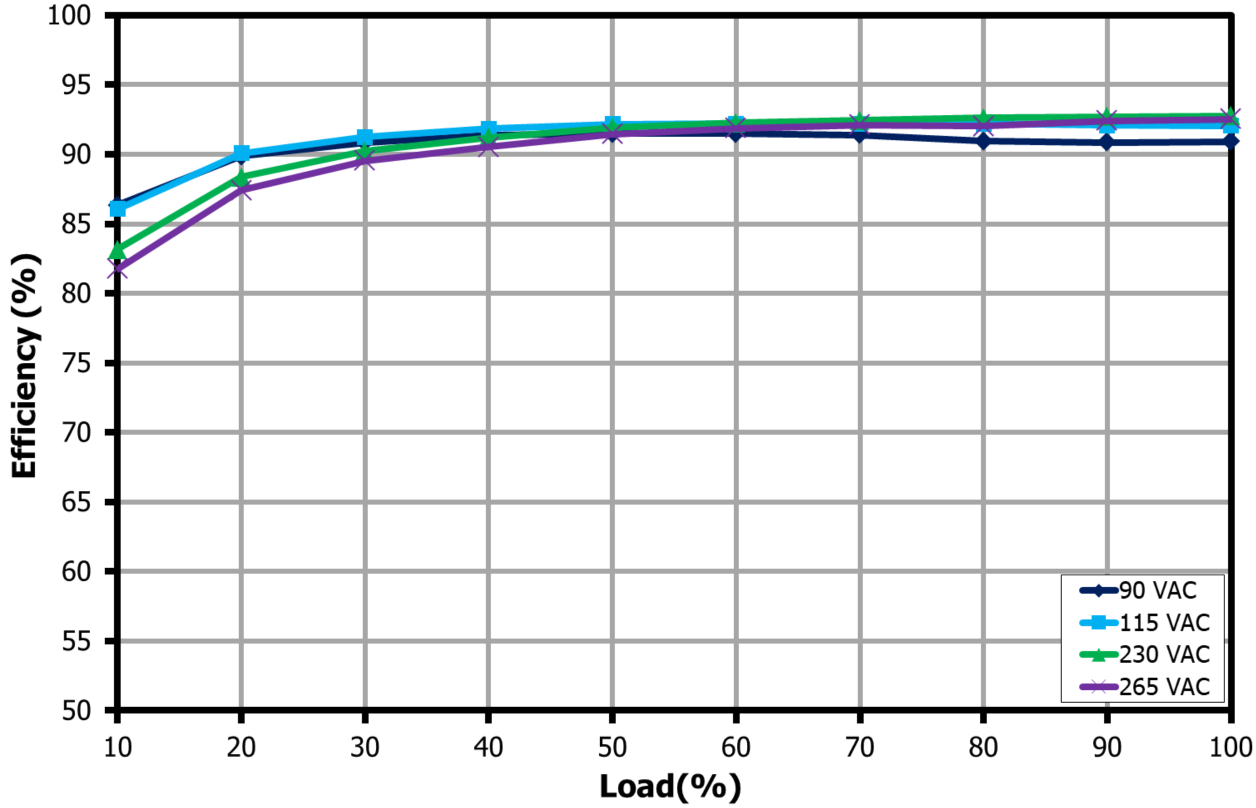

Figure 19 – Efficiency vs. Load for 15 V Output, Room Temperature.

11.5.4 Output: 20 V / 1.5 A

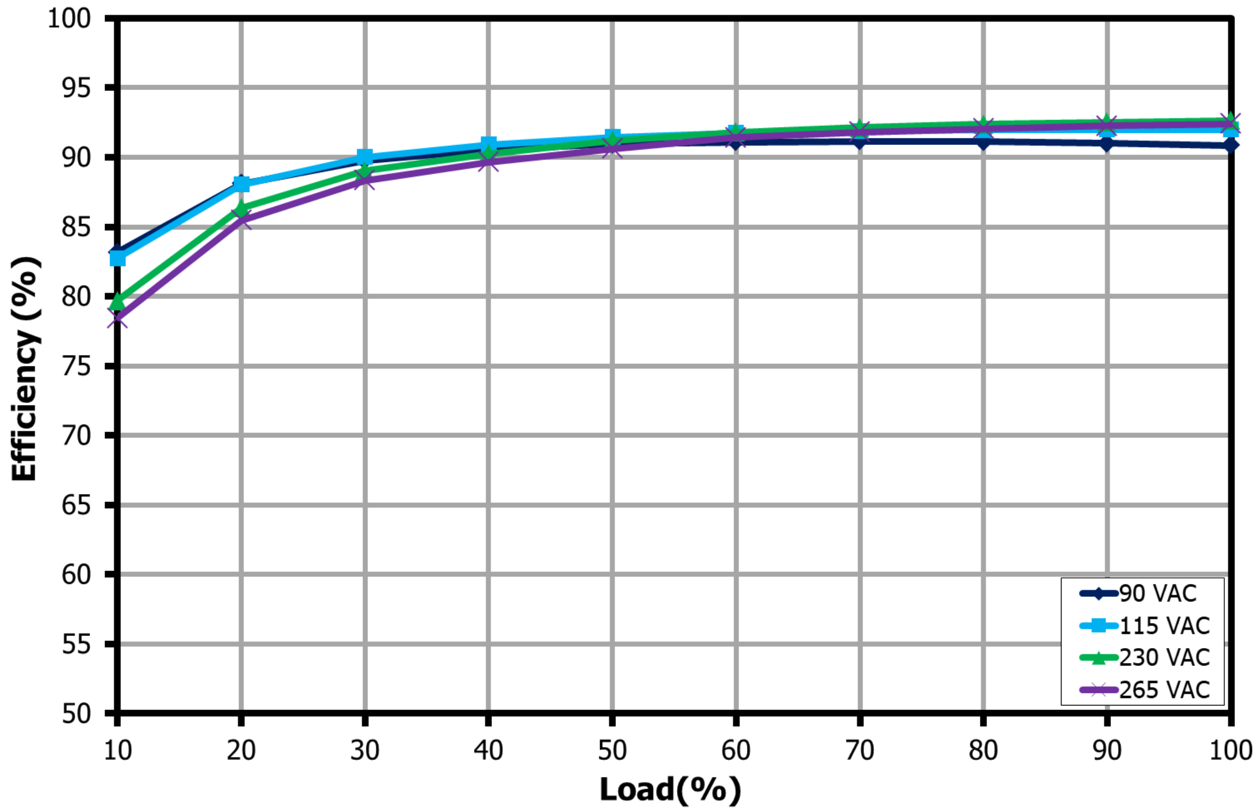

Figure 20 – Efficiency vs. Load for 20 V Output, Room Temperature.

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11.6 ***Load Regulation (On Board)***

11.6.1 Output: 5 V / 3 A

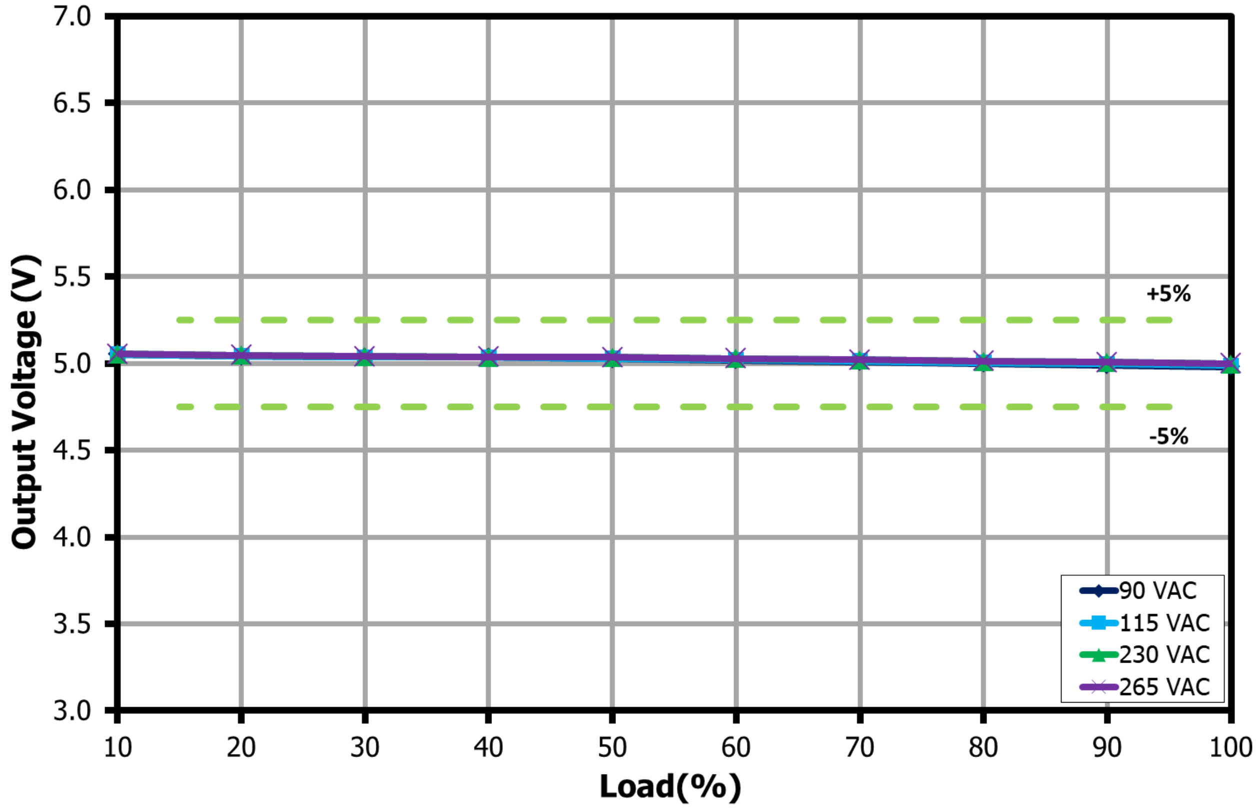

Figure 21 – Output Voltage vs. Output Load for 5 V Output, Room Temperature.

11.6.2 Output: 9 V / 3 A

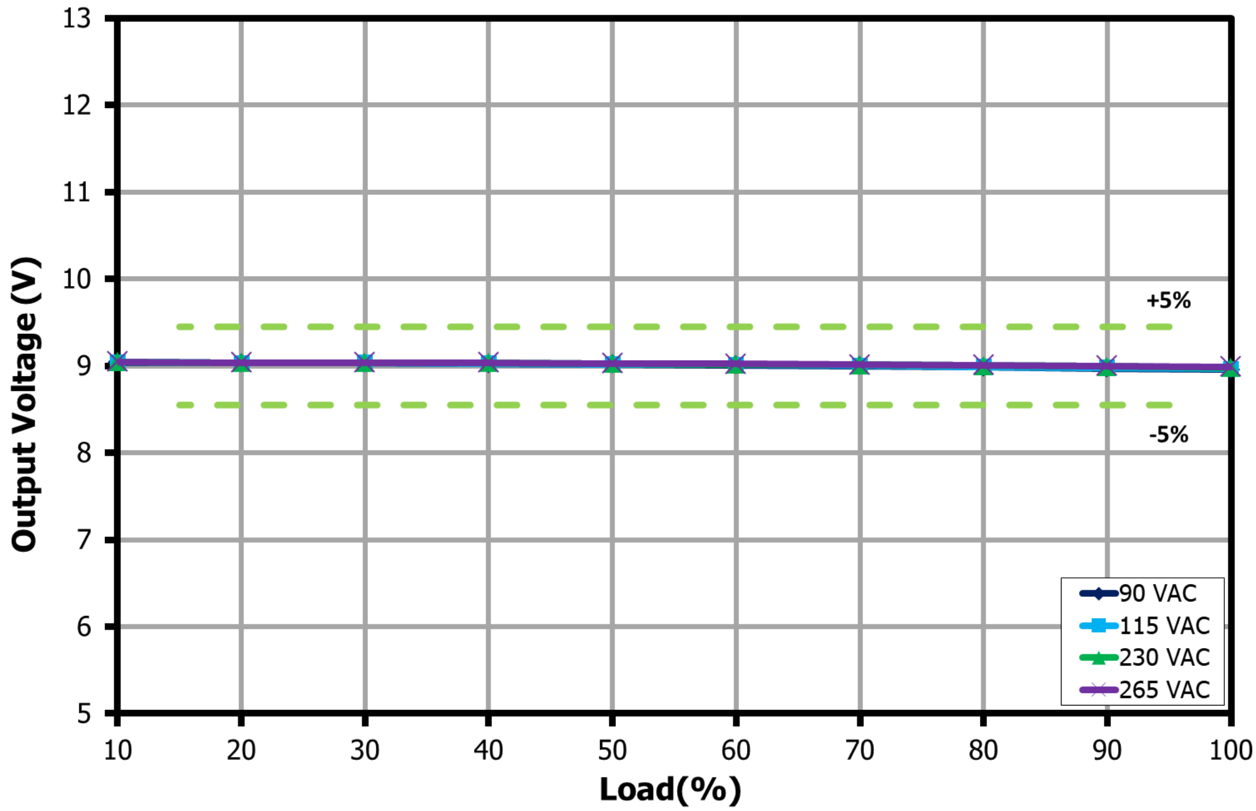

Figure 22 – Output Voltage vs. Output Load for 9 V Output, Room Temperature.

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11.6.3 Output: 15 V / 2 A

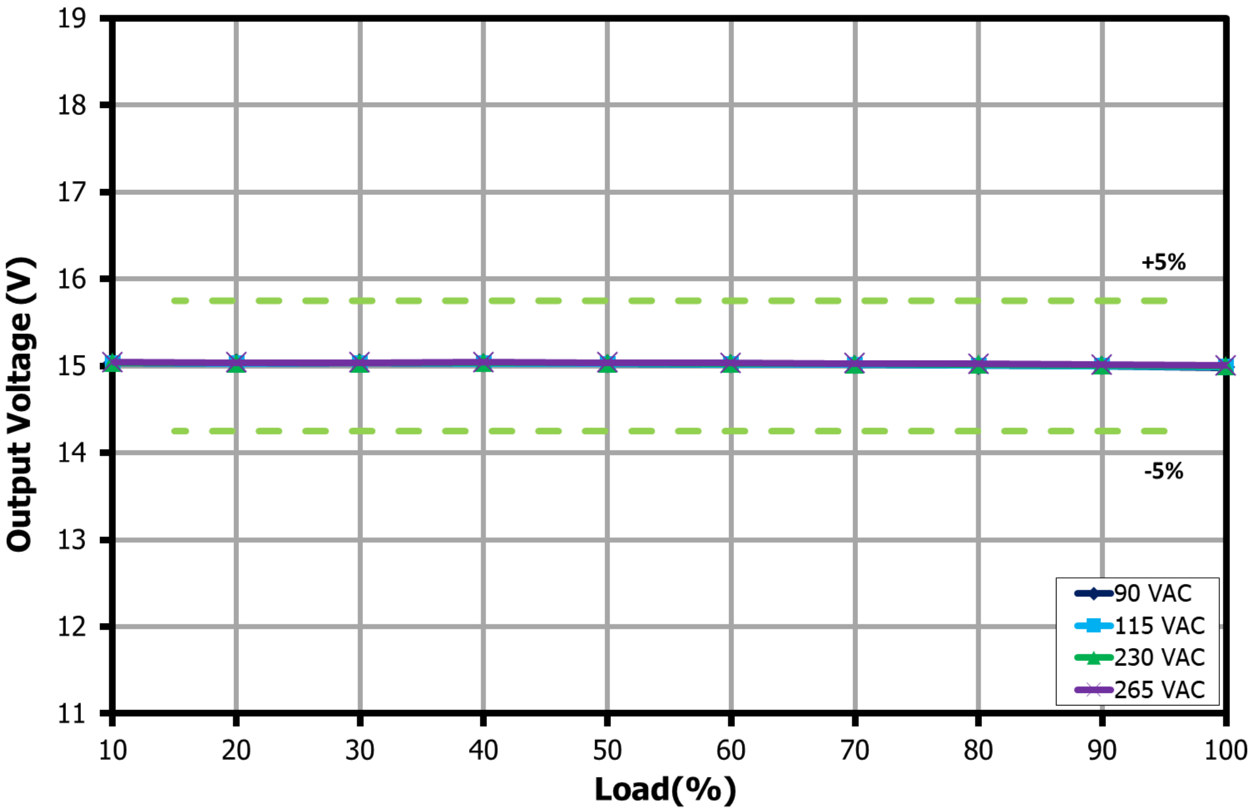

Figure 23 – Output Voltage vs. Output Load for 15 V Output, Room Temperature.

11.6.4 Output: 20 V / 1.5 A

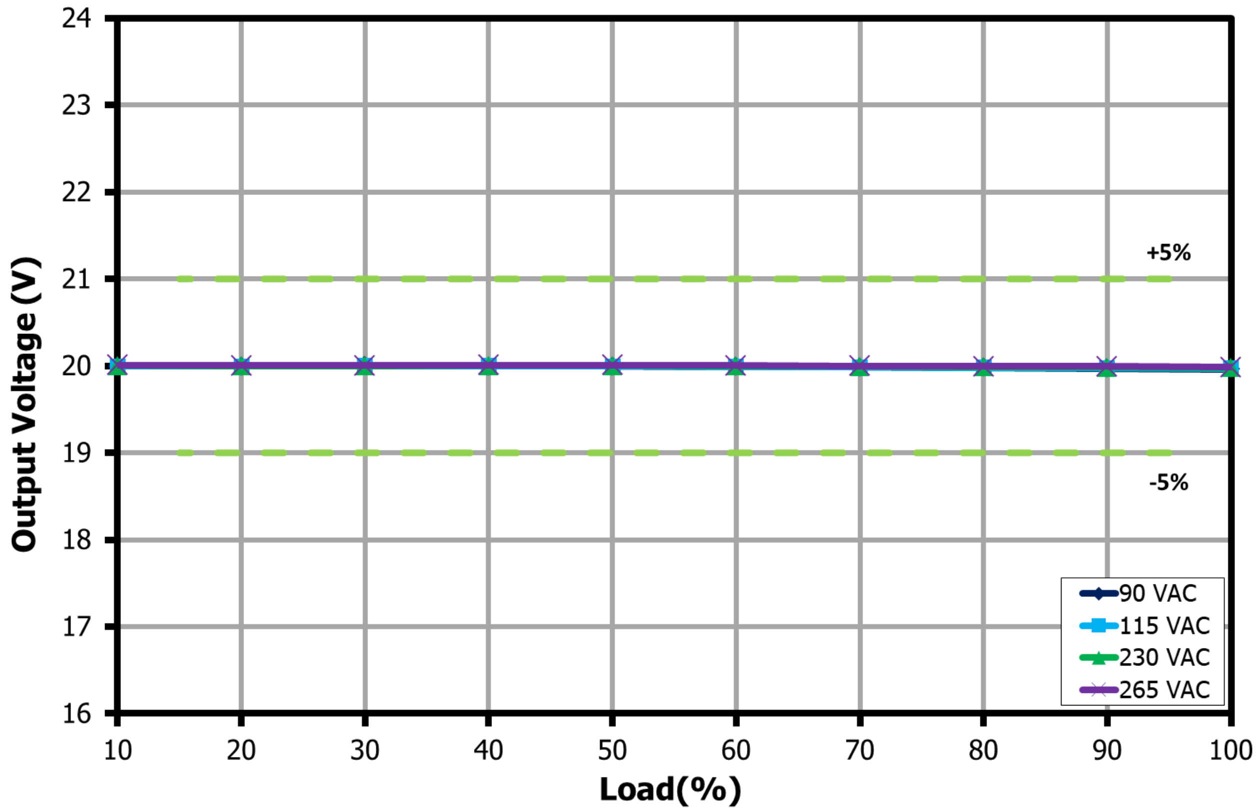

Figure 24 – Output Voltage vs. Output Load for 20 V Output, Room Temperature.

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11.7 ***Line Regulation (On Board)***

11.7.1 Output: 5 V / 3 A

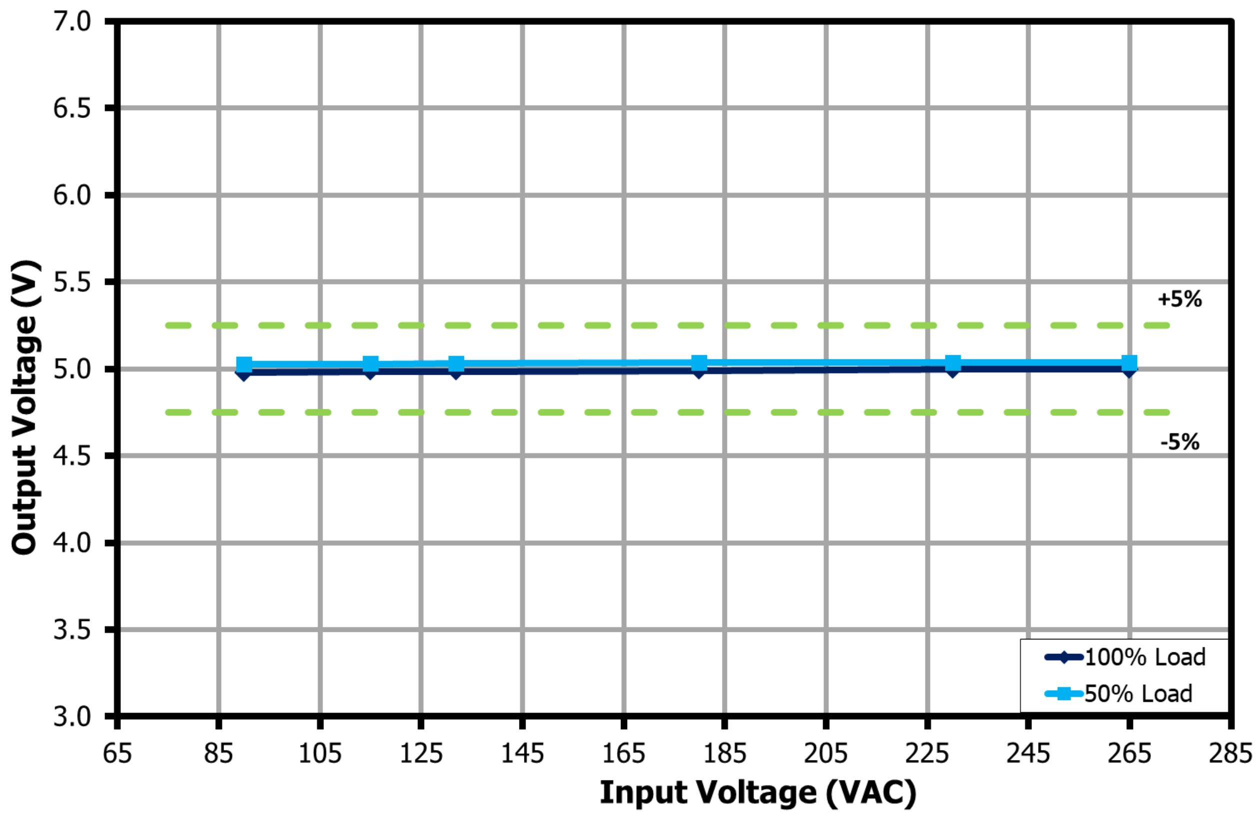

Figure 25 – Output Voltage vs. Input Line Voltage for 5 V Output, Room Temperature.

11.7.2 Output: 9 V / 3 A

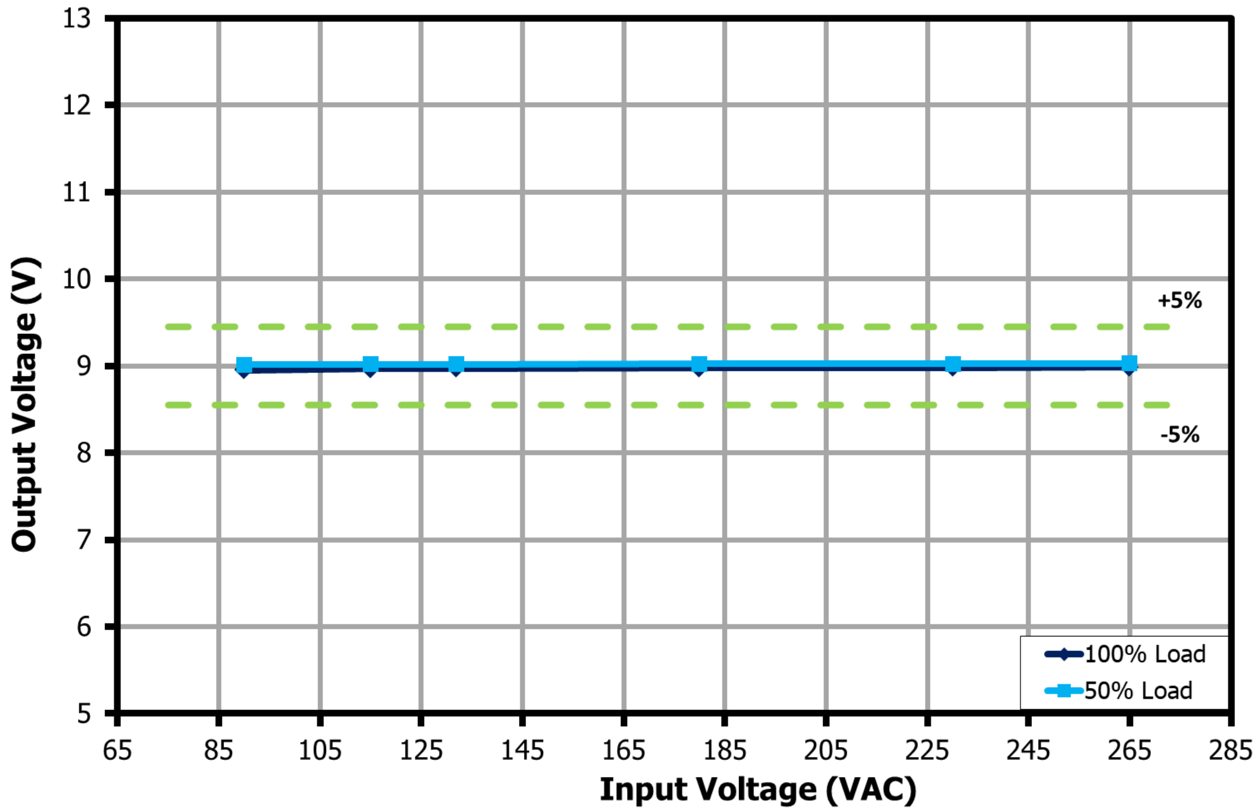

Figure 26 – Output Voltage vs. Input Line Voltage for 9 V Output, Room Temperature.

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11.7.3 Output: 15 V / 2 A

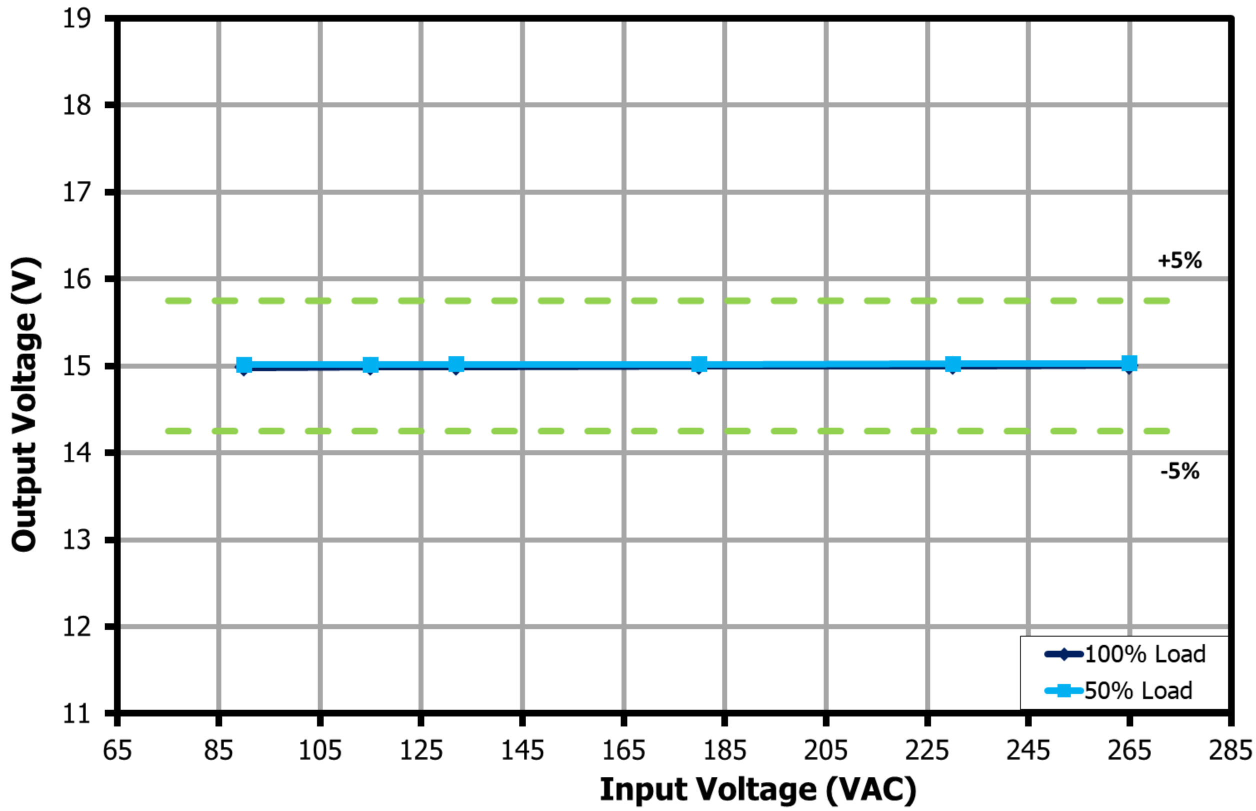

Figure 27 – Output Voltage vs. Input Line Voltage for 15 V Output, Room Temperature.

11.7.4 Output: 20 V / 1.5 A

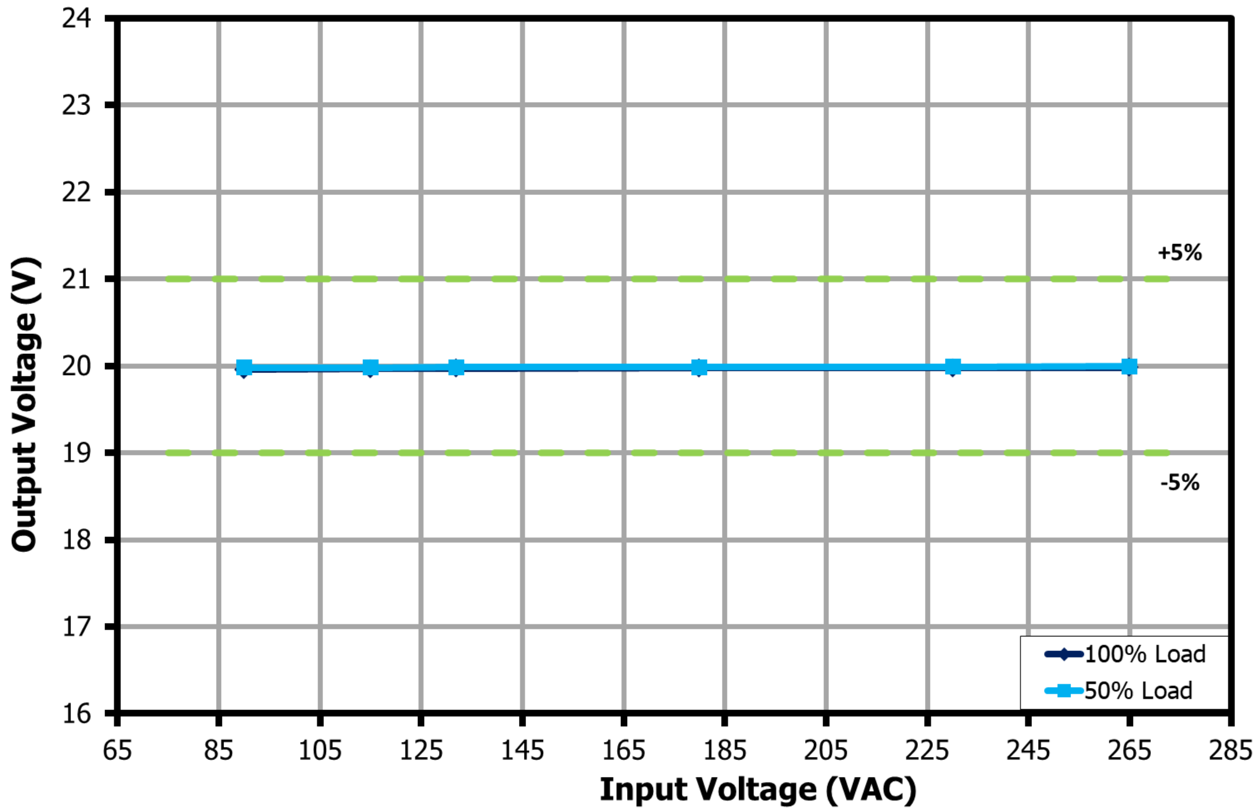

Figure 28 – Output Voltage vs. Input Line Voltage for 20 V Output, Room Temperature.

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12 Thermal Performance

12.1 *Thermal Performance in Open Case, 25 ºC Ambient*

Note: Measurements taken at room temperature ambient (approximately 25 °C).

12.1.1 Output: 5 V / 3 A (90 VAC)

Figure 29 – Top Thermal Image.
Bx1: Transformer, T1 = 47.1 ºC.
Bx2: Thermistor, RT1 = 45.4 ºC.

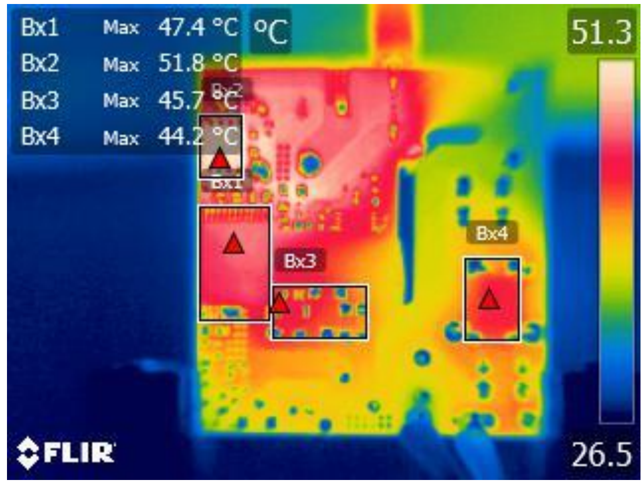

Figure 30 – Bottom Thermal Image.
Bx1: InnoSwitch3-Pro, U2 = 47.4 ºC.
Bx2: SR FET, Q2 = 51.8 ºC.
Bx3: Primary Snubber = 45.7 ºC.
Bx4: Bridge Rectifier, BR1 = 44.2 ºC.

12.1.2 Output: 5 V / 3 A (265 VAC)

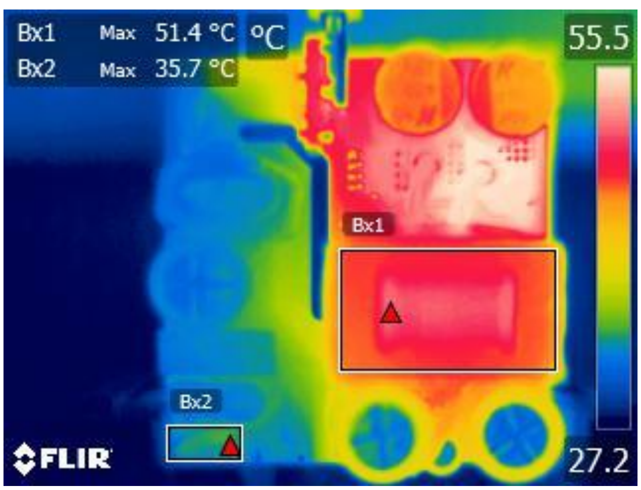

Figure 31 – Top Thermal Image.
Bx1: Transformer, T1 = 51.4 ºC.
Bx2: Thermistor, RT1 = 35.7 ºC.

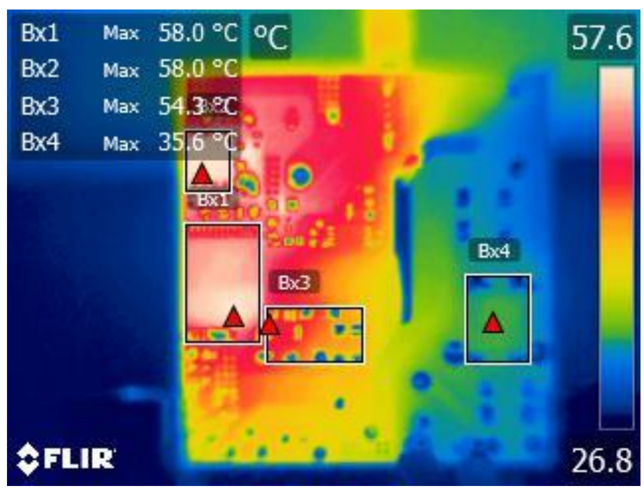

Figure 32 – Bottom Thermal Image.
Bx1: InnoSwitch3-Pro, U2 = 58.0 ºC.
Bx2: SR FET, Q2 = 58.0 ºC.
Bx3: Primary Snubber = 54.3 ºC.
Bx4: Bridge Rectifier, BR1 = 35.7 ºC.

12.1.3 Output: 9 V / 3 A (90 VAC)

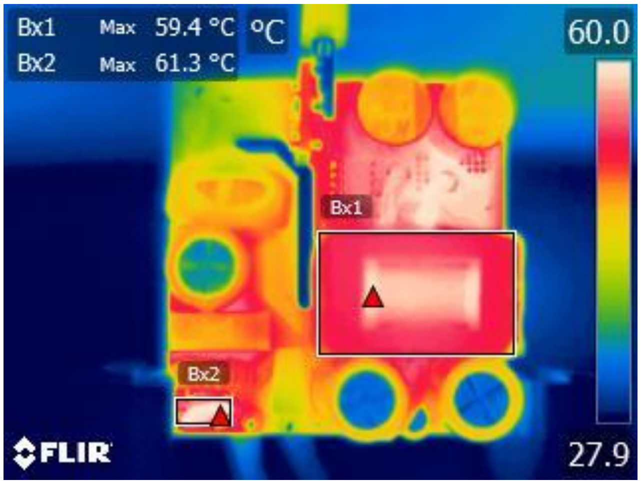

Figure 33 – Top Thermal Image.
Bx1: Transformer, T1 = 59.4 ºC.
Bx2: Thermistor, RT1 = 61.3 ºC.

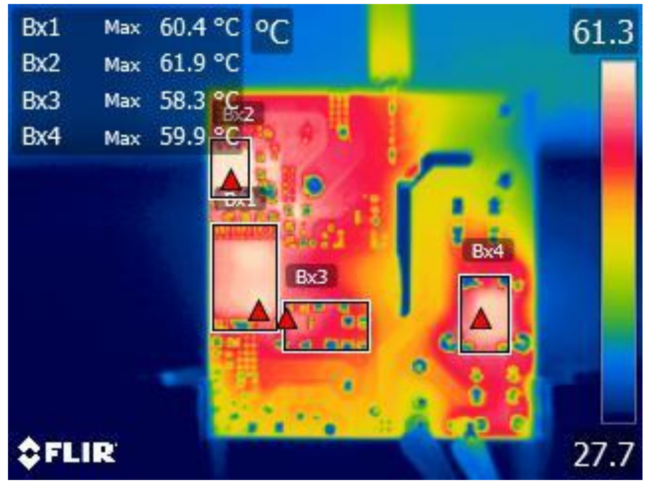

Figure 34 – Bottom Thermal Image.
Bx1: InnoSwitch3-Pro, U2 = 60.4 ºC.
Bx2: SR FET, Q2 = 61.9 ºC.
Bx3: Primary Snubber = 58.3 ºC.
Bx4: Bridge Rectifier, BR1 = 59.9 ºC.

12.1.4 Output: 9 V / 3 A (265 VAC)

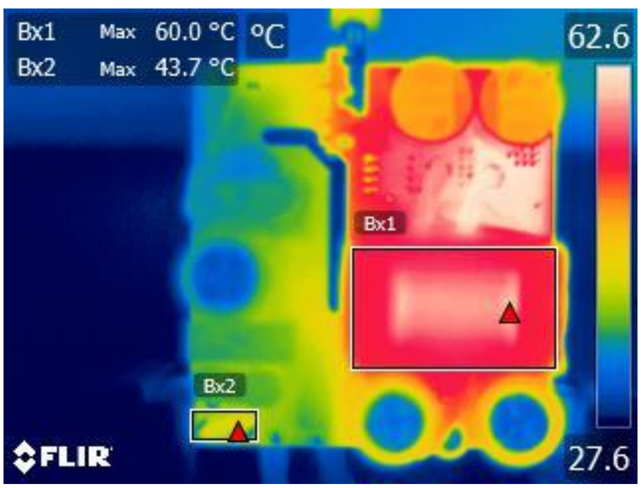

Figure 35 – Top Thermal Image.
Bx1: Transformer, T1 = 60.0 ºC.
Bx2: Thermistor, RT1 = 43.7 ºC.

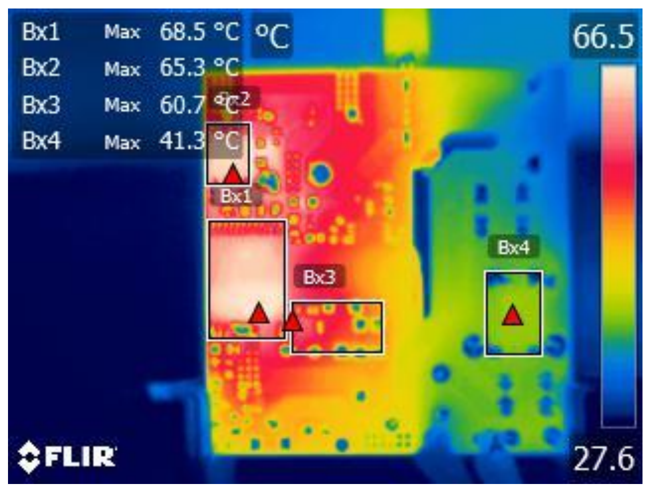

Figure 36 – Bottom Thermal Image.
Bx1: InnoSwitch3-Pro, U2 = 68.5 ºC.
Bx2: SR FET, Q2 = 65.3 ºC.
Bx3: Primary Snubber = 60.7 ºC.
Bx4: Bridge Rectifier, BR1 = 41.3 ºC.

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12.1.5 Output: 15 V / 2 A (90 VAC)

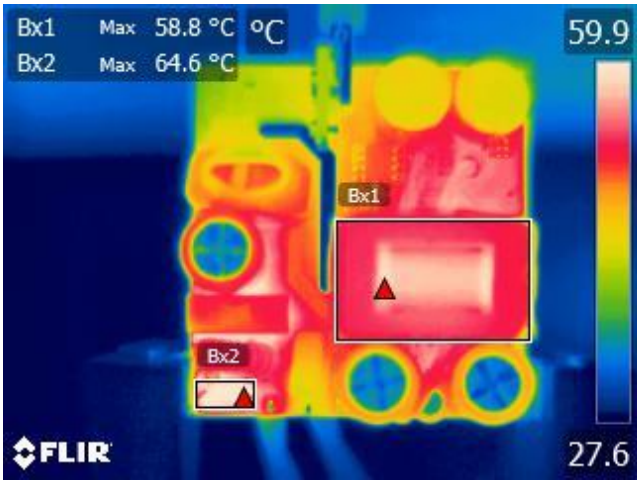

Figure 37 – Top Thermal Image.
Bx1: Transformer, T1 = 58.8 ºC.
Bx2: Thermistor, RT1 = 64.6 ºC.

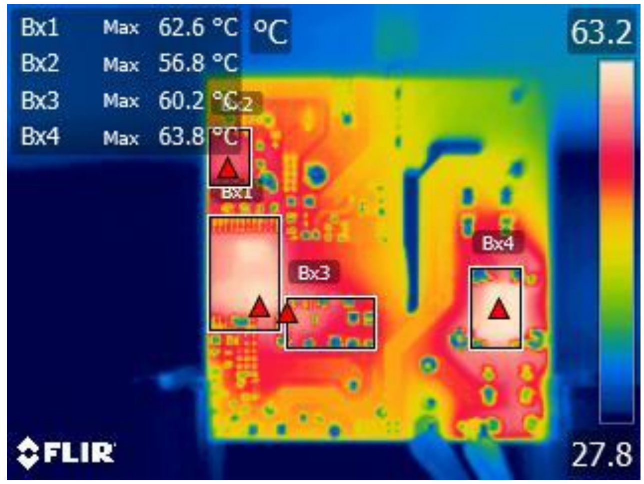

Figure 38 – Bottom Thermal Image.
Bx1: InnoSwitch3-Pro, U2 = 62.6 ºC.
Bx2: SR FET, Q2 = 56.8 ºC.
Bx3: Primary Snubber = 60.2 ºC.
Bx4: Bridge Rectifier, BR1 = 63.8 ºC.

12.1.6 Output: 15 V / 2 A (265 VAC)

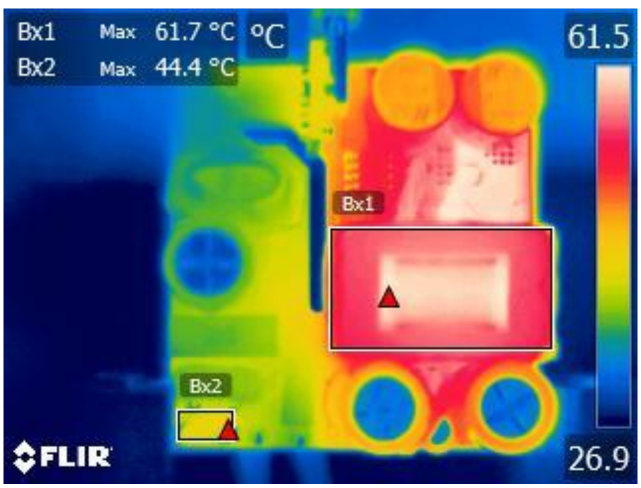

Figure 39 – Top Thermal Image.
Bx1: Transformer, T1 = 61.7 ºC.
Bx2: Thermistor, RT1 = 44.4 ºC.

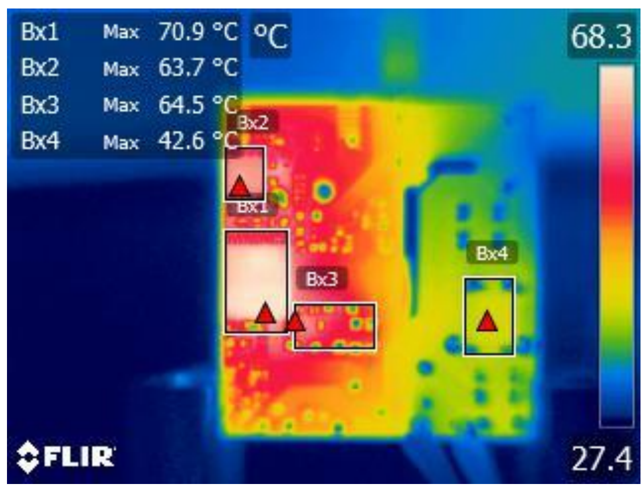

Figure 40 – Bottom Thermal Image.
Bx1: InnoSwitch3-Pro, U2 = 70.9 ºC.
Bx2: SR FET, Q2 = 63.7 ºC.
Bx3: Primary Snubber = 64.5 ºC.
Bx4: Bridge Rectifier, BR1 = 42.6 ºC.

12.1.7 Output: 20 V / 1.5 A (90 VAC)

Figure 41 – Top Thermal Image.
Bx1: Transformer, T1 = 61.4 ºC.
Bx2: Thermistor, RT1 = 65.8 ºC.

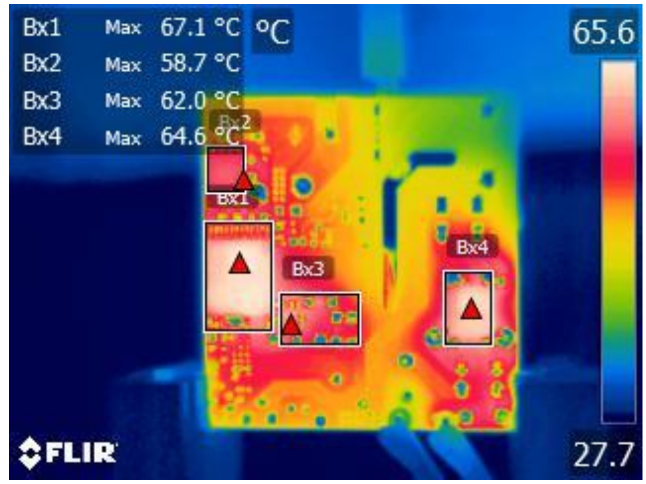

Figure 42 – Bottom Thermal Image.
Bx1: InnoSwitch3-Pro, U2 = 67.1 ºC.
Bx2: SR FET, Q2 = 58.7 ºC.
Bx3: Primary Snubber = 62.0 ºC.
Bx4: Bridge Rectifier, BR1 = 64.6 ºC.

12.1.8 Output: 20 V / 1.5 A (265 VAC)

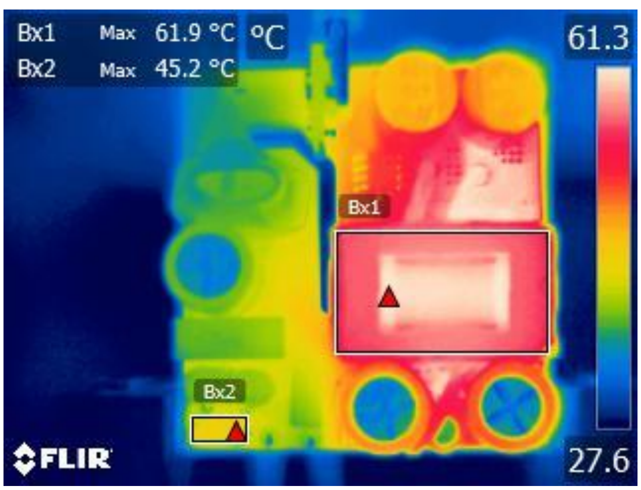

Figure 43 – Top Thermal Image.
Bx1: Transformer, T1 = 61.9 ºC.
Bx2: Thermistor, RT1 = 45.2 ºC.

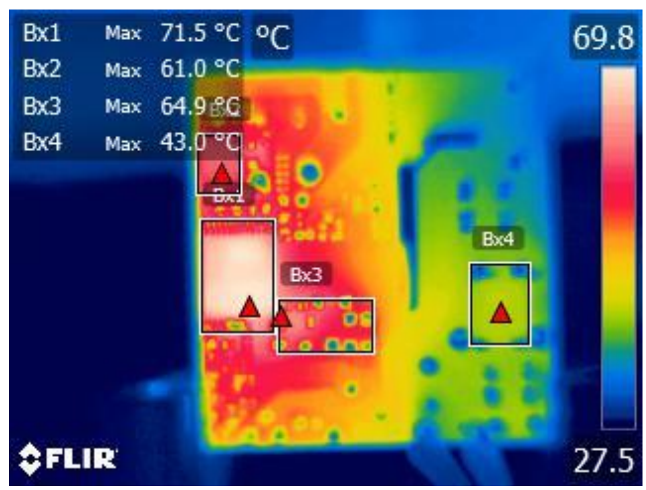

Figure 44 – Bottom Thermal Image.
Bx1: InnoSwitch3-Pro, U2 = 71.5 ºC.
Bx2: SR FET, Q2 = 61.0 ºC.
Bx3: Primary Snubber = 64.9 ºC.
Bx4: Bridge Rectifier, BR1 = 43.0 ºC.

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12.2 *Thermal Performance in Open Case, 45 ºC Ambient*

Note: Measurements taken using Type-T thermocouple and with the board inside a thermal chamber.

12.2.1 Components Temperature Summary

Condition	Component	Temperature (°C)			
		15 V / 2 A (90 VAC)	15 V / 2 A (265 VAC)	20 V / 1.5 A (90 VAC)	20 V / 1.5 A (265 VAC)
Open Frame Unit, 45°C Ambient	RT1	74.2	60.0	73.5	60.8
	BR1	78.7	62.3	79.6	62.9
	INN3378C	81.3	84.3	82.3	85.3
	SRFET	77.9	80.9	77.6	81.1
	T1-core	72.7	73.8	73.1	74.9
	T1-wire	76.6	77.5	76.8	78.2
	CLAMP	69.8	70.2	71.1	71.8
	PASSFET	71.1	70.6	70.6	70.1
	VP302	69.1	69.0	69.5	69.4
	AMBIENT	47.1	46.9	47.3	47.4

12.2.2 Output: 15 V / 2 A (90 VAC)

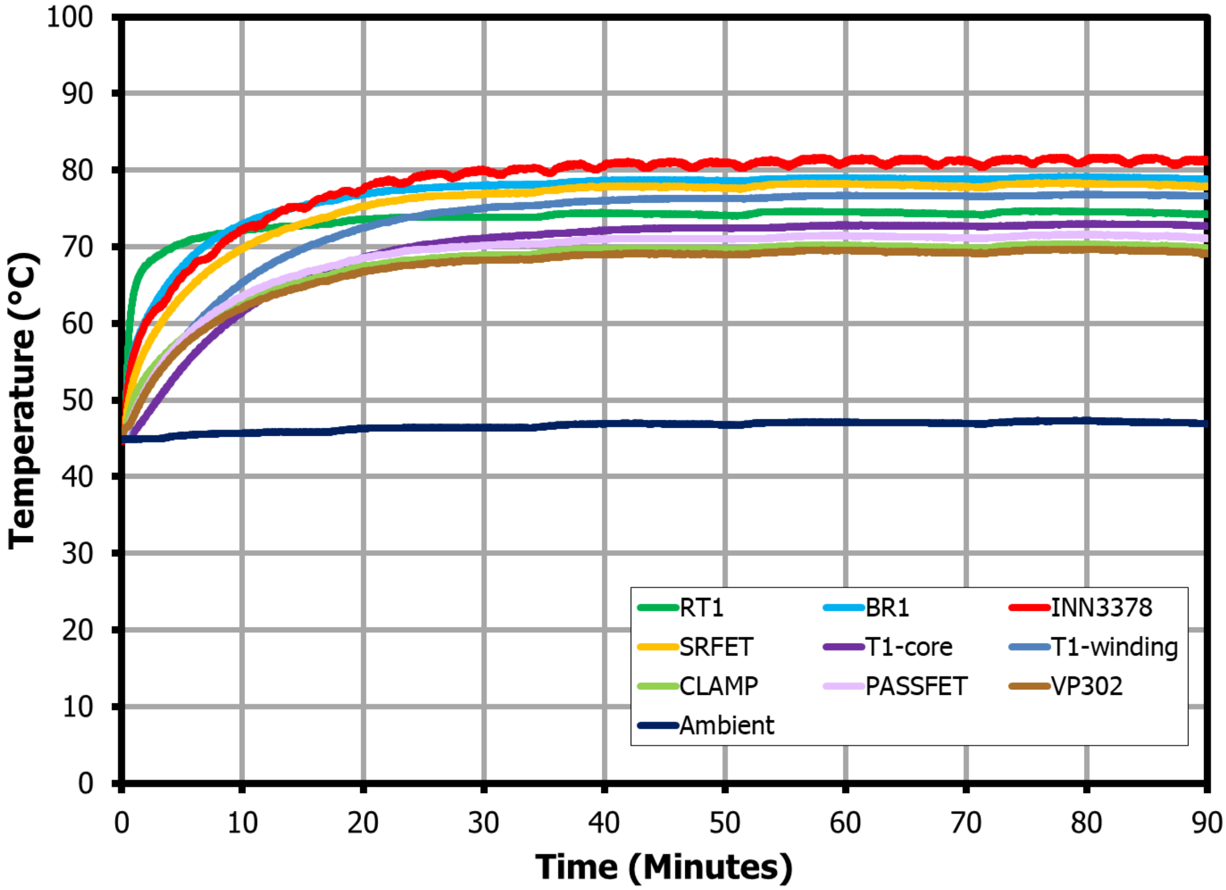

Figure 45 – Enclosed Unit Thermal Performance at 15 V / 2 A Output, 90 VAC, 45 °C Ambient.

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12.2.3 Output: 15 V / 2 A (265 VAC)

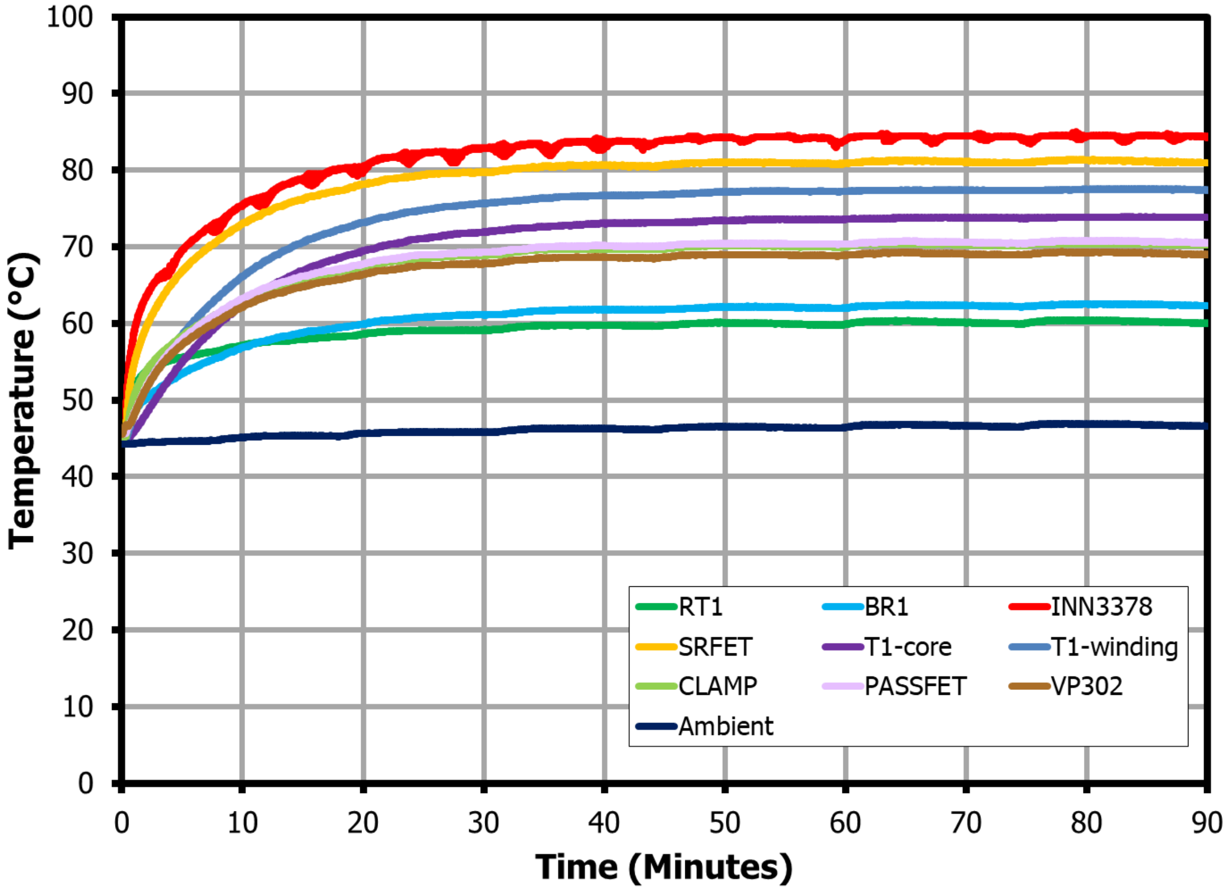

Figure 46 – Enclosed Unit Thermal Performance at 15 V / 2 A Output, 265 VAC, 45 °C Ambient.

12.2.4 Output: 20 V / 1.5 A (90 VAC)

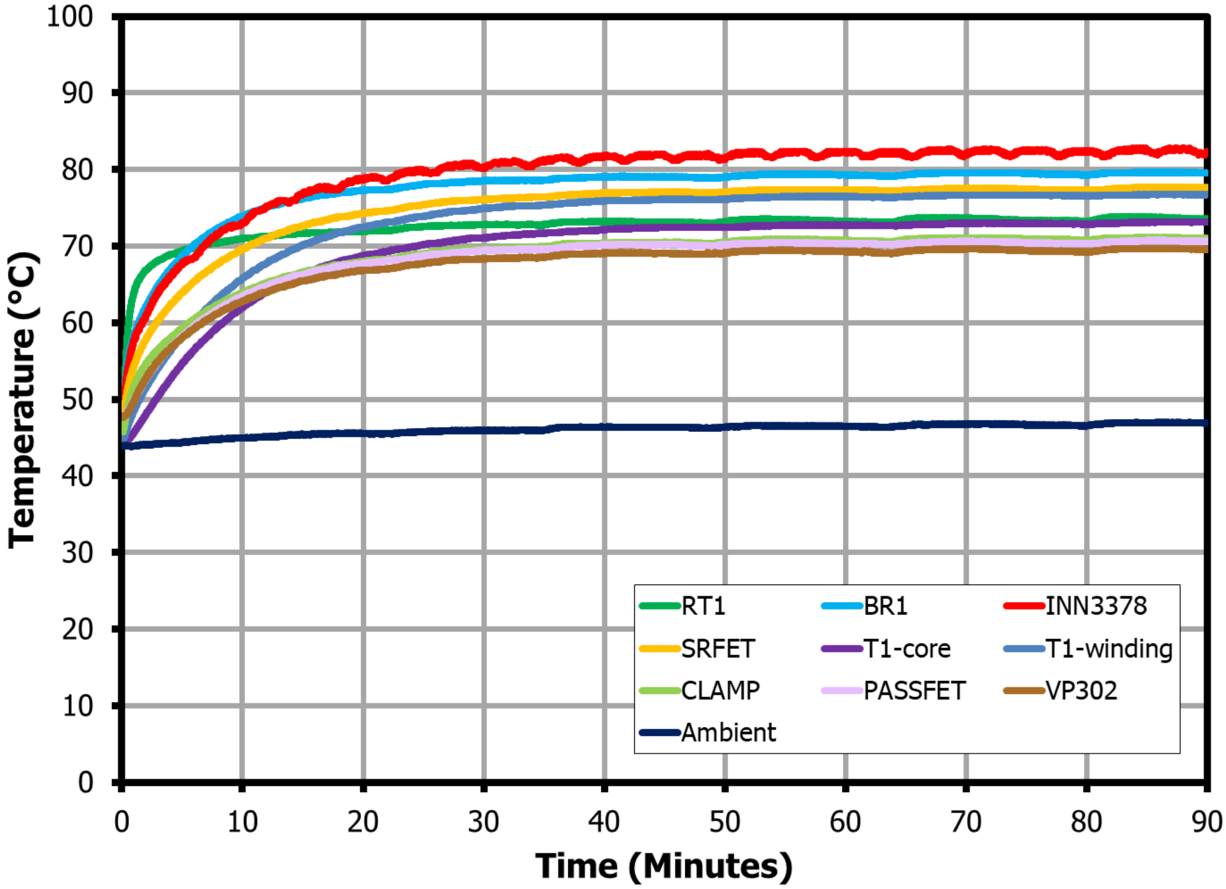

Figure 47 – Enclosed Unit Thermal Performance at 20 V / 1.5 A Output, 90 VAC, 45 °C Ambient.

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12.2.5 Output: 20 V / 1.5 A (265 VAC)

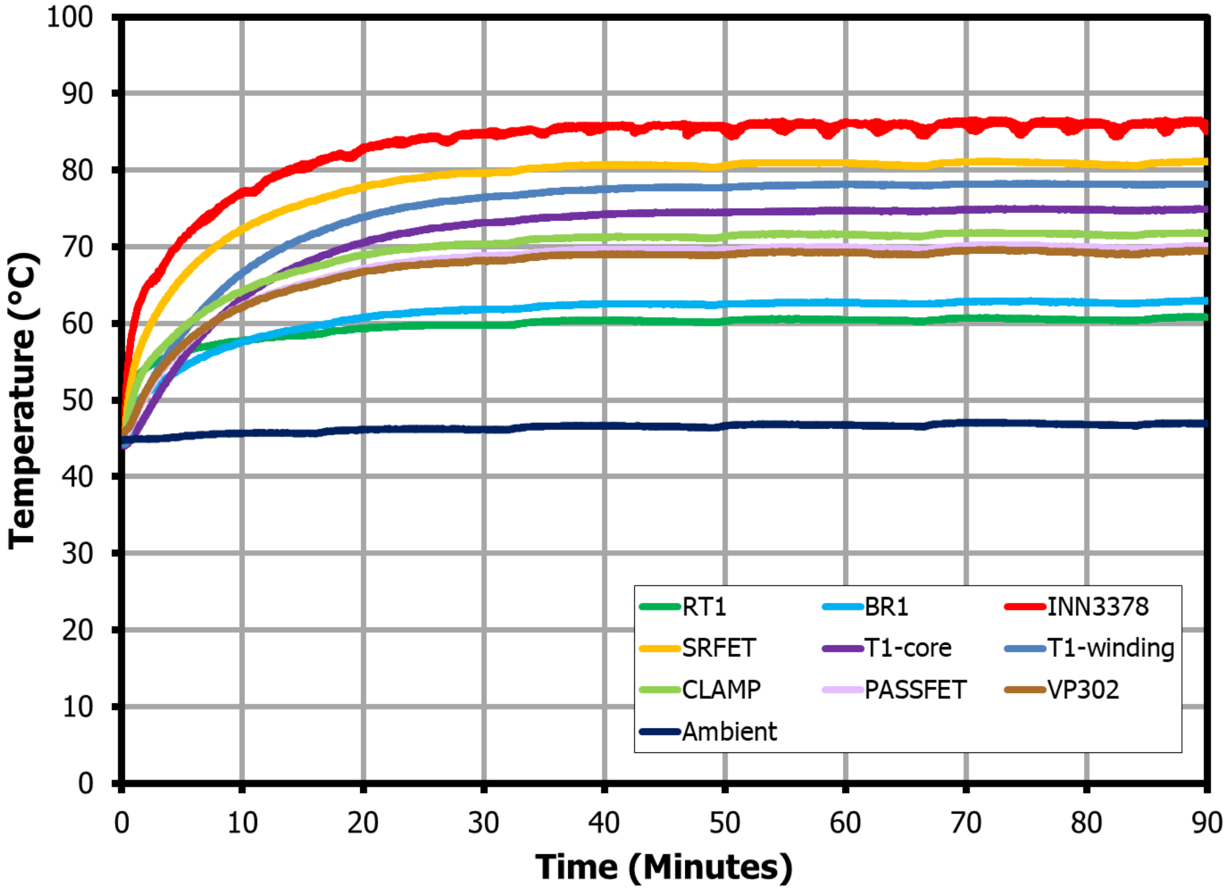

Figure 48 – Enclosed Unit Thermal Performance at 20 V / 1.5 A Output, 265 VAC, 45 °C Ambient.

13 Waveforms

Note: Waveforms taken at room temperature ambient (approximately 25 °C)

13.1 ***Start-up Waveforms***

13.1.1 Output Voltage and Current

Note: Output voltage waveforms captured at the end of 100 mΩ cable.

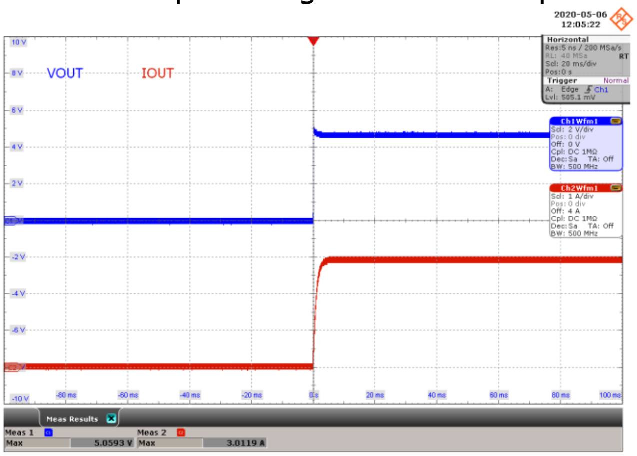

Figure 49 – Output Voltage and Current.
90 VAC, 5.0 V, 3 A Load (CR mode).
V_{OUT} = 5.059 V maximum.
CH1: V_{OUT}, 2 V / div.
CH2: I_{LOAD}, 1 A / div.
Time: 20 ms / div.

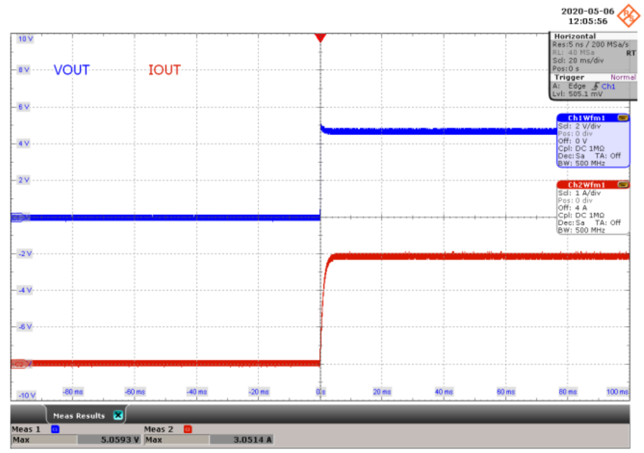

Figure 50 – Output Voltage and Current.
265 VAC, 5.0 V, 3 A Load (CR mode).
V_{OUT} = 5.059 V maximum.
CH1: V_{OUT}, 2 V / div.
CH2: I_{LOAD}, 1 A / div.
Time: 20 ms / div.

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13.1.2 Primary Drain Voltage and Current

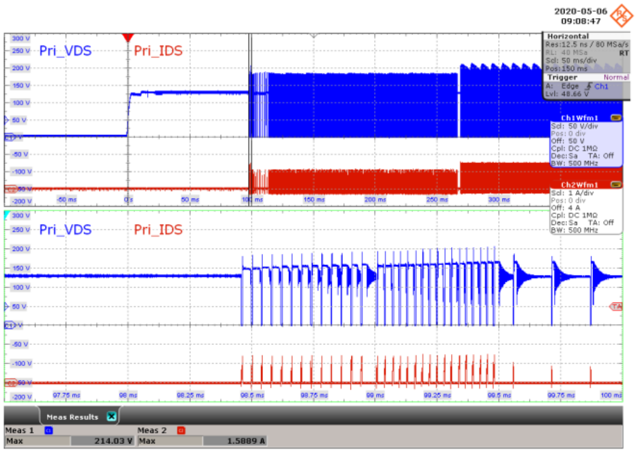

Figure 51 – Primary Drain Voltage and Current.
90 VAC, 5.0 V, 3 A Load.
V_{DS_PRI} = 214 V maximum.
CH1: V_{DS_PRI}, 50 V / div.
CH2: I_{DS_PRI}, 1 A / div.
Time: 50 ms / div. (250 µs / div. zoom)

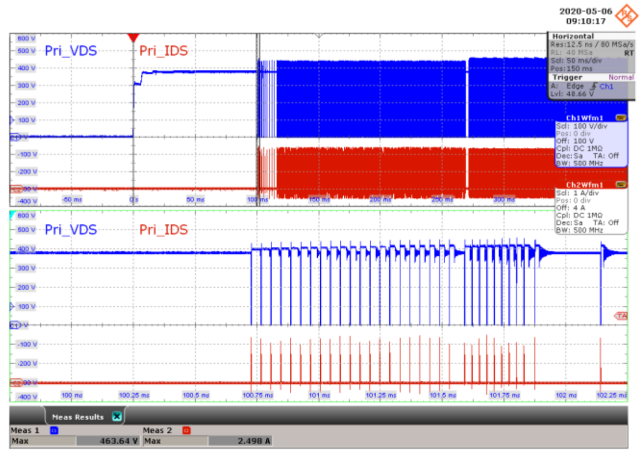

Figure 52 – Primary Drain Voltage and Current.
265 VAC, 5.0 V, 3 A Load.
V_{DS_PRI} = 463 V maximum.
CH1: V_{DS_PRI}, 100 V / div.
CH2: I_{DS_PRI}, 1 A / div.
Time: 50 ms / div. (250 µs / div. zoom)

13.1.3 SR FET Drain Voltage and Current

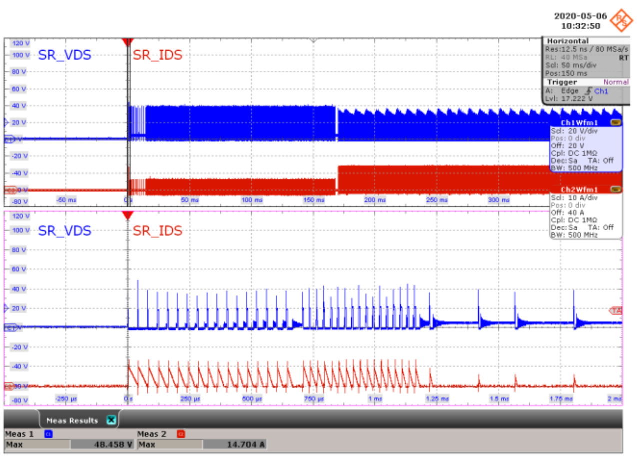

Figure 53 – SR FET Drain Voltage and Current.
90 VAC, 5.0 V, 3 A Load.
V_{DS_SRFET} = 48.4 V maximum.
CH1: V_{DS_SRFET}, 20 V / div.
CH2: I_{DS_SRFET}, 10 A / div.
Time: 50 ms / div. (250 µs / div. zoom)

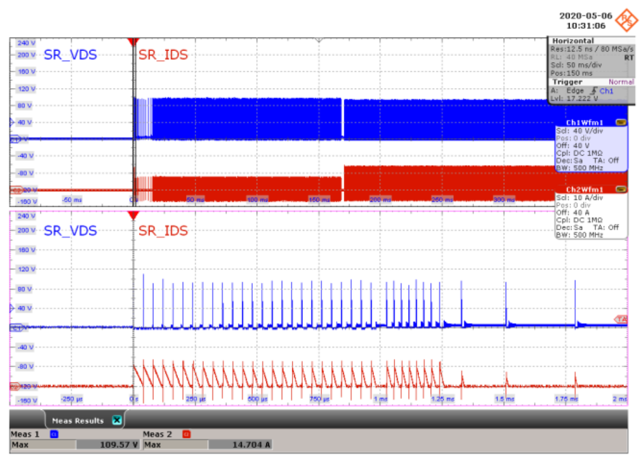

Figure 54 – SR FET Drain Voltage and Current.
265 VAC, 5.0 V, 3 A Load.
V_{DS_SRFET} = 109 V maximum.
CH1: V_{DS_SRFET}, 40 V / div.
CH2: I_{DS_SRFET}, 10 A / div.
Time: 50 ms / div. (250 µs / div. zoom)

13.2 ***Primary Drain Voltage and Current (Steady-State)***

13.2.1 Output: 5 V / 3 A

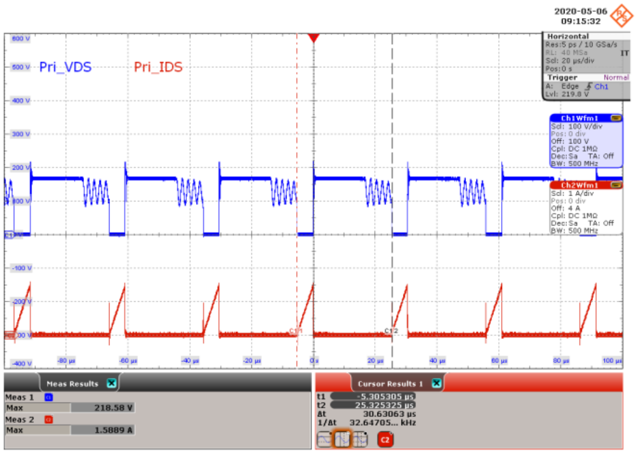

Figure 55 – Primary Drain Voltage and Current.
90 VAC, 5.0 V, 3 A Load.
V_{DS_PRI} = 218 V maximum.
CH1: V_{DS_PRI}, 100 V / div.
CH2: I_{DS_PRI}, 1 A / div.
Time: 20 μs / div.

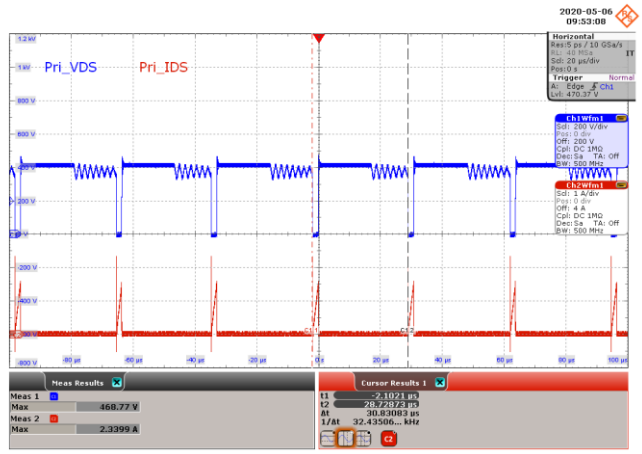

Figure 56 – Primary Drain Voltage and Current.
265 VAC, 5.0 V, 3 A Load.
V_{DS_PRI} = 468 V maximum.
CH1: V_{DS_PRI}, 200 V / div.
CH2: I_{DS_PRI}, 1 A / div.
Time: 20 μs / div.

13.2.2 Output: 9 V / 3 A

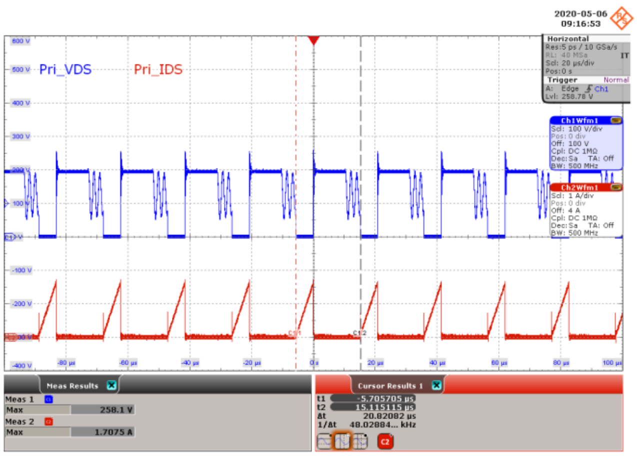

Figure 57 – Primary Drain Voltage and Current.
90 VAC, 9.0 V, 3 A Load.
V_{DS_PRI} = 258 V maximum.
CH1: V_{DS_PRI}, 100 V / div.
CH2: I_{DS_PRI}, 1 A / div.
Time: 20 μs / div.

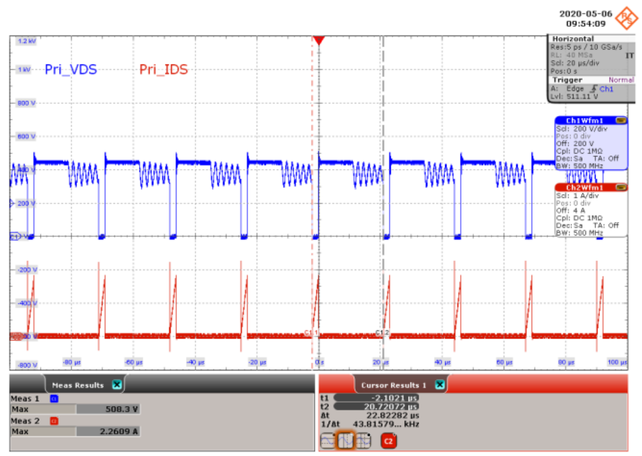

Figure 58 – Primary Drain Voltage and Current.
265 VAC, 9.0 V, 3 A Load.
V_{DS_PRI} = 508 V maximum.
CH1: V_{DS_PRI}, 200 V / div.
CH2: I_{DS_PRI}, 1 A / div.
Time: 20 μs / div.

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13.2.3 Output: 15 V / 2 A

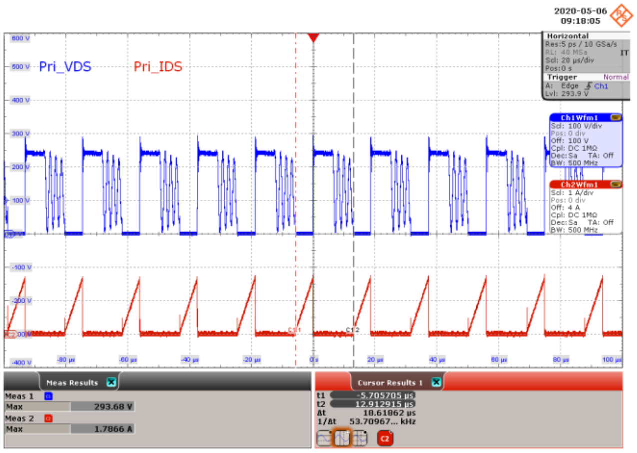

Figure 59 – Primary Drain Voltage and Current.
90 VAC, 15.0 V, 2 A Load.
V_{DS_PRI} = 293 V maximum.
CH1: V_{DS_PRI}, 100 V / div.
CH2: I_{DS_PRI}, 1 A / div.
Time: 20 µs / div.

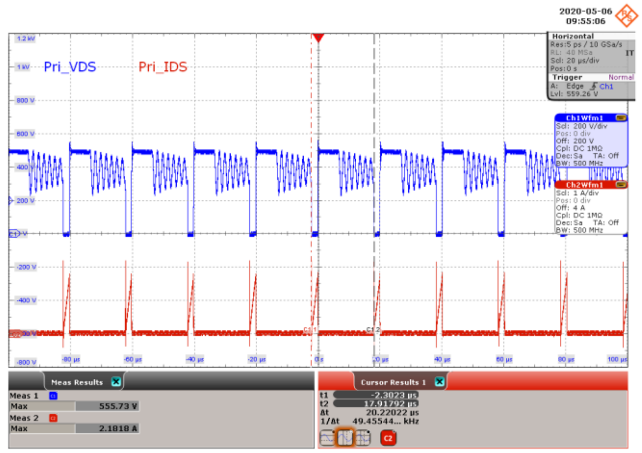

Figure 60 – Primary Drain Voltage and Current.
265 VAC, 15.0 V, 2 A Load.
V_{DS_PRI} = 555 V maximum.
CH1: V_{DS_PRI}, 200 V / div.
CH2: I_{DS_PRI}, 1 A / div.
Time: 20 µs / div.

13.2.4 Output: 20 V / 1.5 A

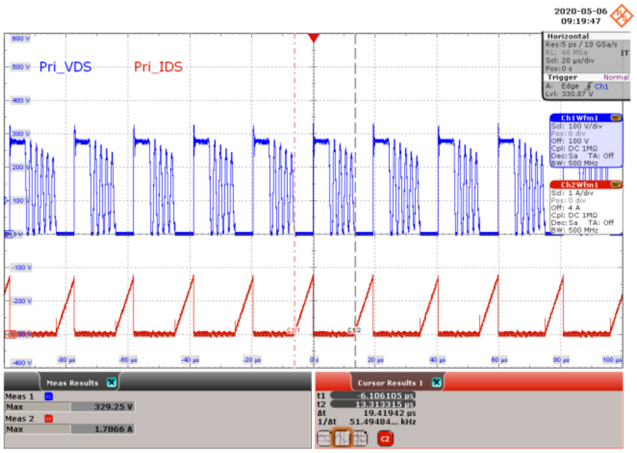

Figure 61 – Primary Drain Voltage and Current.
90 VAC, 20.0 V, 1.5 A Load.
V_{DS_PRI} = 329 V maximum.
CH1: V_{DS_PRI}, 100 V / div.
CH2: I_{DS_PRI}, 1 A / div.
Time: 20 µs / div.

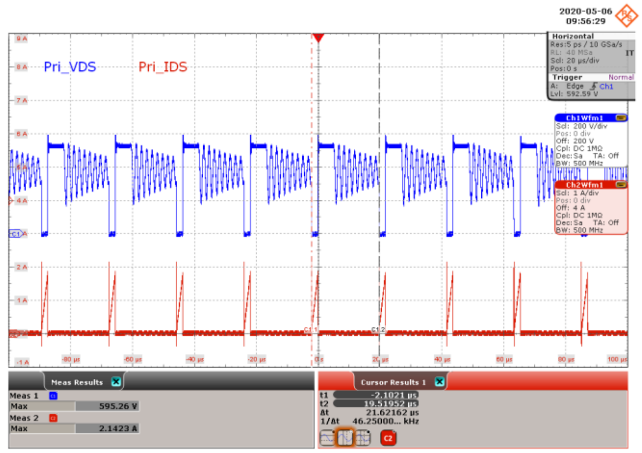

Figure 62 – Primary Drain Voltage and Current.
265 VAC, 20.0 V, 1.5 A Load.
V_{DS_PRI} = 595 V maximum.
CH1: V_{DS_PRI}, 200 V / div.
CH2: I_{DS_PRI}, 1 A / div.
Time: 20 µs / div.

13.3 ***SR FET Drain Voltage and Current (Steady-State)***

13.3.1 Output: 5 V / 3 A

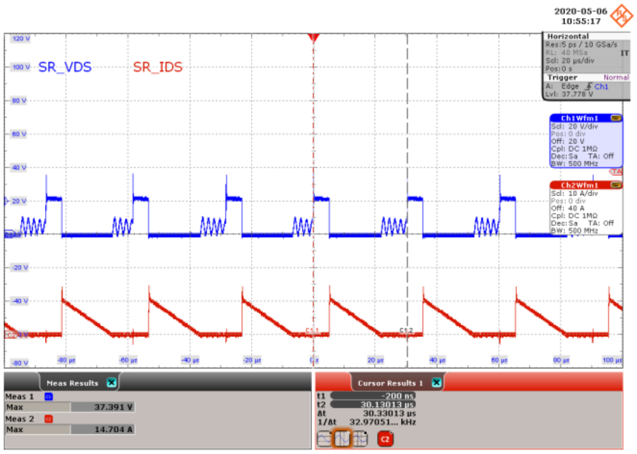

Figure 63 – SR FET Drain Voltage and Current.
90 VAC, 5.0 V, 3 A Load.
V_{DS_SRFET} = 37.3 V maximum.
CH1: V_{DS_SRFET}, 20 V / div.
CH2: I_{DS_SRFET}, 10 A / div.
Time: 20 µs / div.

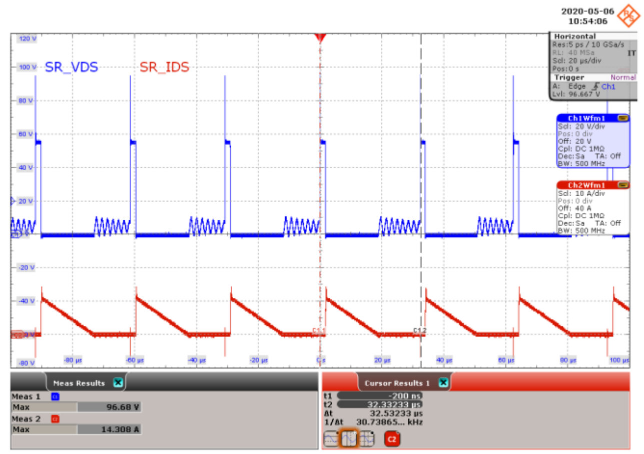

Figure 64 – SR FET Drain Voltage and Current.
265 VAC, 5.0 V, 3 A Load.
V_{DS_SRFET} = 96.6 V maximum.
CH1: V_{DS_SRFET}, 20 V / div.
CH2: I_{DS_SRFET}, 10 A / div.
Time: 20 µs / div.

13.3.2 Output: 9 V / 3 A

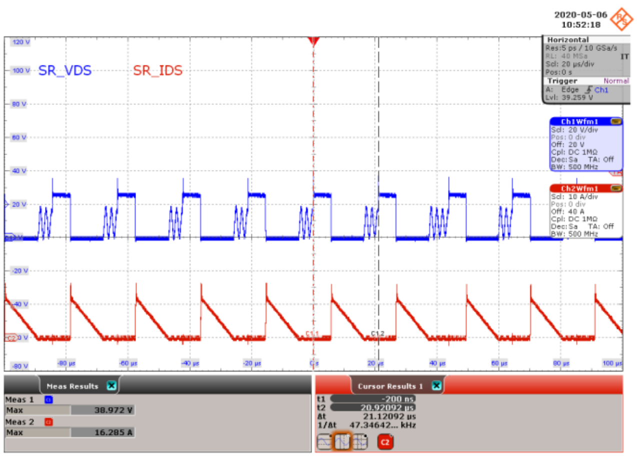

Figure 65 – SR FET Drain Voltage and Current.
90 VAC, 9.0 V, 3 A Load.
V_{DS_SRFET} = 38.9 V maximum.
CH1: V_{DS_SRFET}, 20 V / div.
CH2: I_{DS_SRFET}, 10 A / div.
Time: 20 µs / div.

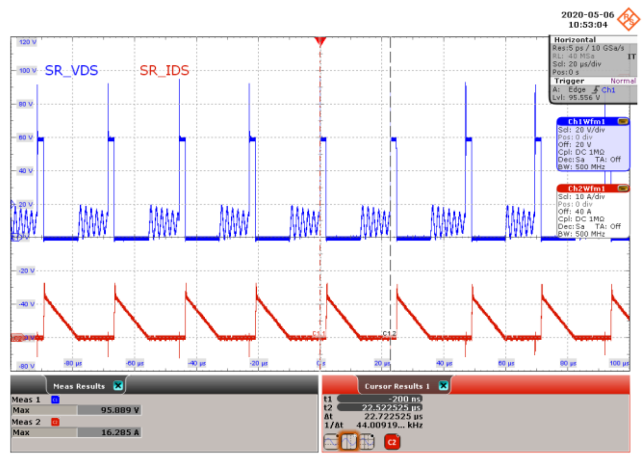

Figure 66 – SR FET Drain Voltage and Current.
265 VAC, 9.0 V, 3 A Load.
V_{DS_SRFET} = 95.8 V maximum.
CH1: V_{DS_SRFET}, 20 V / div.
CH2: I_{DS_SRFET}, 10 A / div.
Time: 20 µs / div.

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13.3.3 Output: 15 V / 2 A

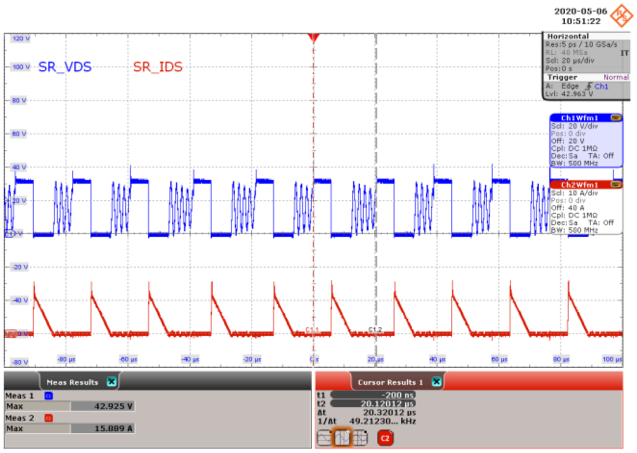

Figure 67 – SR FET Drain Voltage and Current.
90 VAC, 15.0 V, 2 A Load.
V_{DS_SRFET} = 42.9 V maximum.
CH1: V_{DS_SRFET}, 20 V / div.
CH2: I_{DS_SRFET}, 10 A / div.
Time: 20 µs / div.

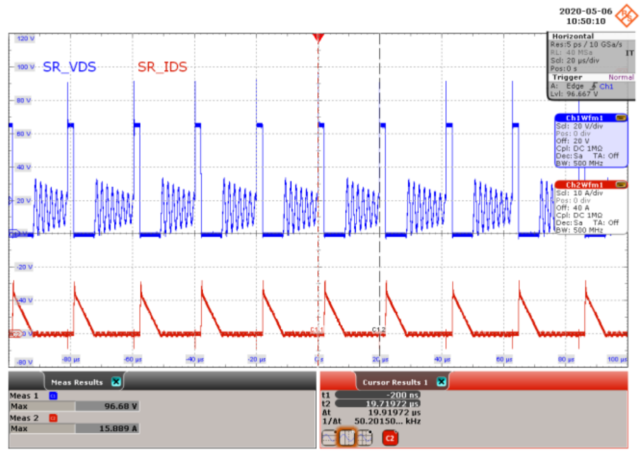

Figure 68 – SR FET Drain Voltage and Current.
265 VAC, 15.0 V, 2 A Load.
V_{DS_SRFET} = 96.6 V maximum.
CH1: V_{DS_SRFET}, 20 V / div.
CH2: I_{DS_SRFET}, 10 A / div.
Time: 20 µs / div.

13.3.4 Output: 20 V / 1.5 A

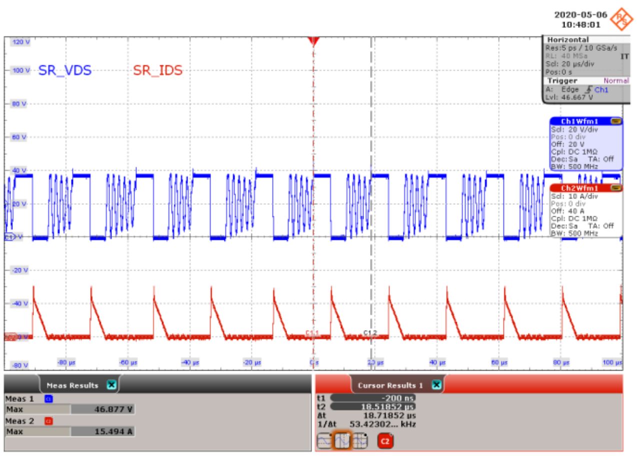

Figure 69 – SR FET Drain Voltage and Current.
90 VAC, 20.0 V, 1.5 A Load.
V_{DS_SRFET} = 46.8 V maximum.
CH1: V_{DS_SRFET}, 20 V / div.
CH2: I_{DS_SRFET}, 10 A / div.
Time: 20 µs / div.

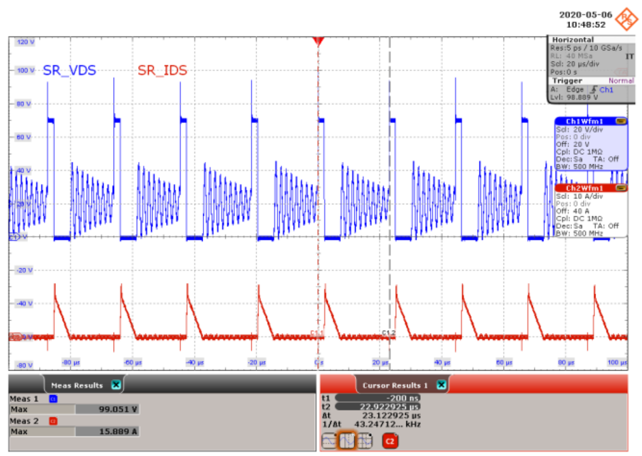

Figure 70 – SR FET Drain Voltage and Current.
265 VAC, 20.0 V, 1.5 A Load.
V_{DS_SRFET} = 99.0 V maximum.
CH1: V_{DS_SRFET}, 20 V / div.
CH2: I_{DS_SRFET}, 10 A / div.
Time: 20 µs / div.

13.4 ***Primary and SR FET Drain Voltage and Current (during Output Voltage Transition)***

13.4.1 Primary Drain Voltage and Current, 3.3 V to 21 V Transition / 1.5 A Load

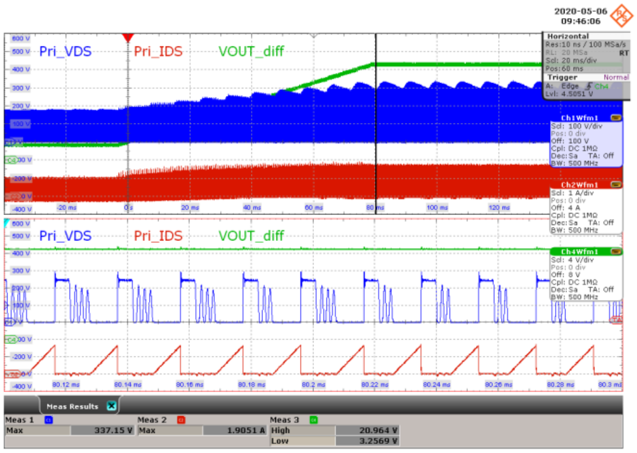

Figure 71 – Primary Drain Voltage and Current.
90 VAC, 3.3 V to 21 V V_{OUT} Transition,
2.25 A Load.
V_{DS_PRI} = 337 V maximum.
CH1: V_{DS_PRI}, 100 V / div.
CH2: I_{DS_PRI}, 1 A / div.
CH4: V_{OUT}, 4 V / div.
Time: 20 ms / div. (20 µs / div. zoom)

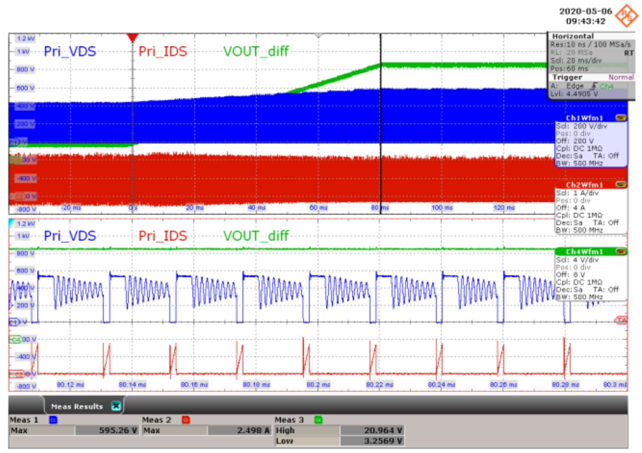

Figure 72 – Primary Drain Voltage and Current.
265 VAC, 3.3 V to 21 V V_{OUT} Transition,
2.25 A Load.
V_{DS_PRI} = 595 V maximum.
CH1: V_{DS_PRI}, 200 V / div.
CH2: I_{DS_PRI}, 1 A / div.
CH4: V_{OUT}, 4 V / div.
Time: 20 ms / div. (20 µs / div. zoom)

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13.4.2 SR FET Drain Voltage and Current, 3.3 V to 21 V Transition / 1.5 A Load

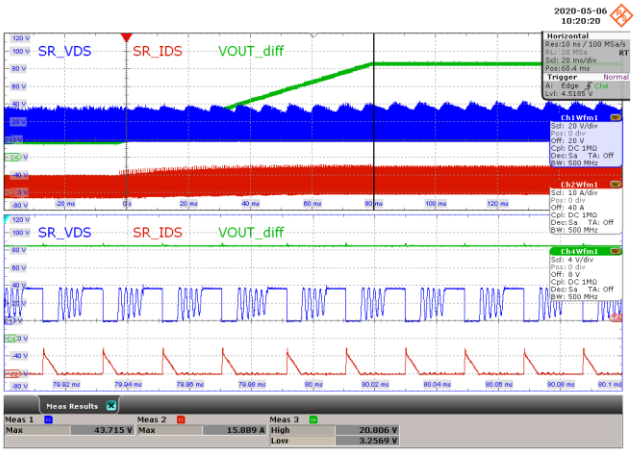

Figure 73 – Primary Drain Voltage and Current.
90 VAC, 3.3 V to 21 V V_{OUT} Transition,
2.25 A Load.
V_{DS_SRFET} = 43.7 V maximum.
CH1: V_{DS_SRFET}, 20 V / div.
CH2: I_{DS_SRFET}, 10 A / div.
CH4: V_{OUT}, 4 V / div.
Time: 20 ms / div. (20 μs / div. zoom)

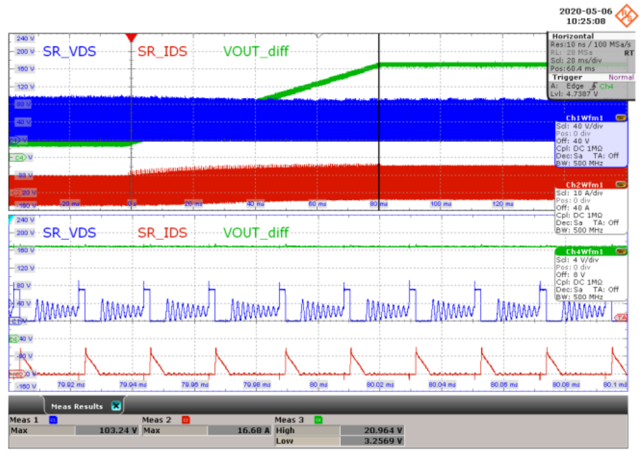

Figure 74 – Primary Drain Voltage and Current.
265 VAC, 3.3 V to 21 V V_{OUT} Transition,
2.25 A Load.
V_{DS_SRFET} = 103.2 V maximum.
CH1: V_{DS_SRFET}, 40 V / div.
CH2: I_{DS_SRFET}, 10 A / div.
CH4: V_{OUT}, 4 V / div.
Time: 20 ms / div. (20 μs / div. zoom)

13.5 ***Load Transient and Output Ripple Measurements***

13.5.1 Ripple Measurement Technique

For load transient response and DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 47 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

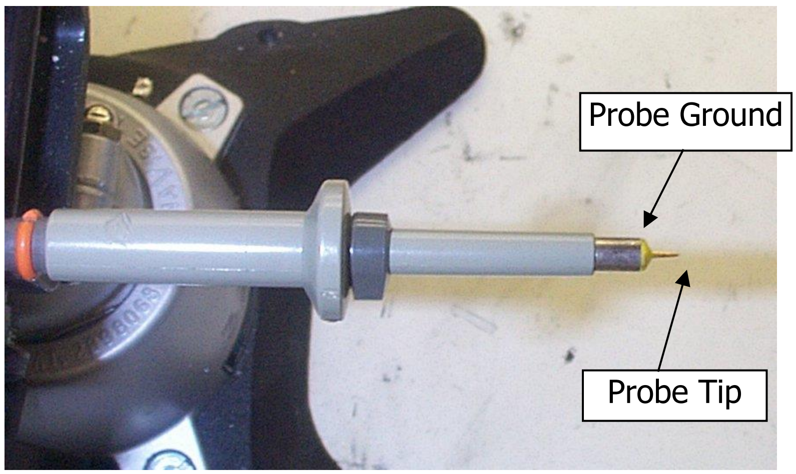

Figure 75 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

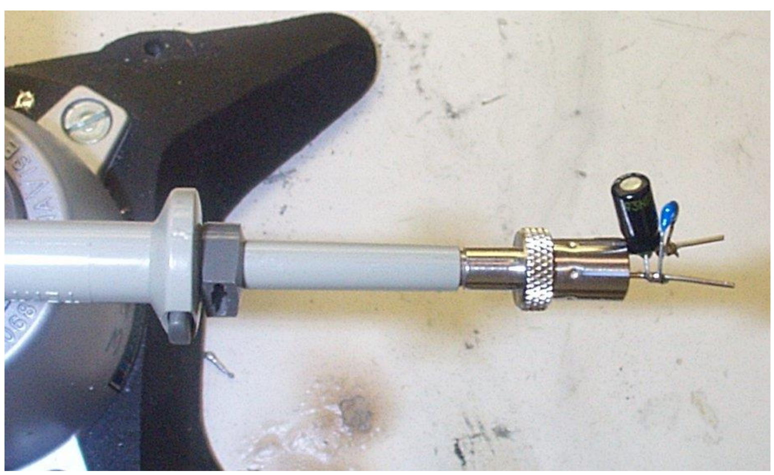

Figure 76 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

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13.6 *Load Transient Response*

Note: 1. Output voltage waveforms captured at the end of 100 mΩ cable using the ripple measurement probe with decoupling capacitors.
2. Duration for load states (high = 5 ms; low = 5 ms) are chosen to show steady-state for each load condition.
3. Load slew rate (150 mA / µs) is based on USB PD 3.0 PPS specification.

13.6.1 Output: 5 V / 3 A

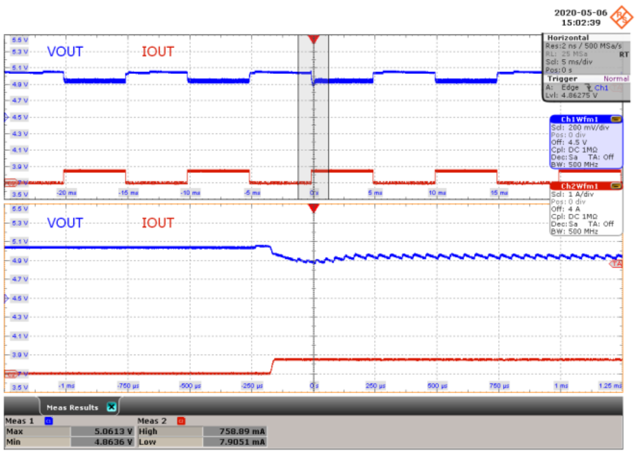

Figure 77 – Transient Response.
90 VAC, 5.0 V, 0 to 25% Load.
V_{OUT} = 5.06 V max, 4.86 V min.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 5 ms / div. (250 µs / div. zoom)

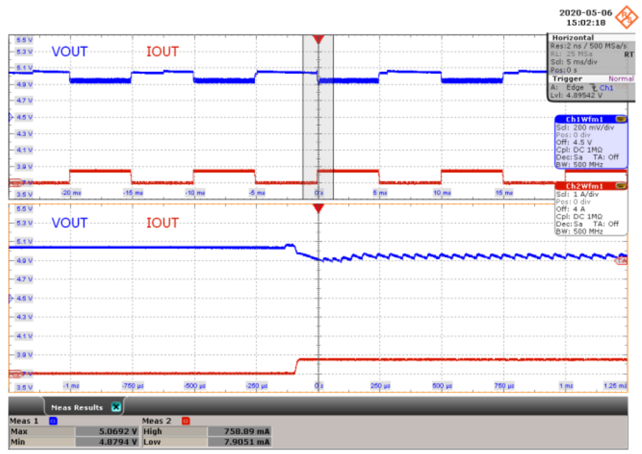

Figure 78 – Transient Response.
265 VAC, 5.0 V, 0 to 25% Load.
V_{OUT} = 5.06 V max, 4.87 V min.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 5 ms / div. (250 µs / div. zoom)

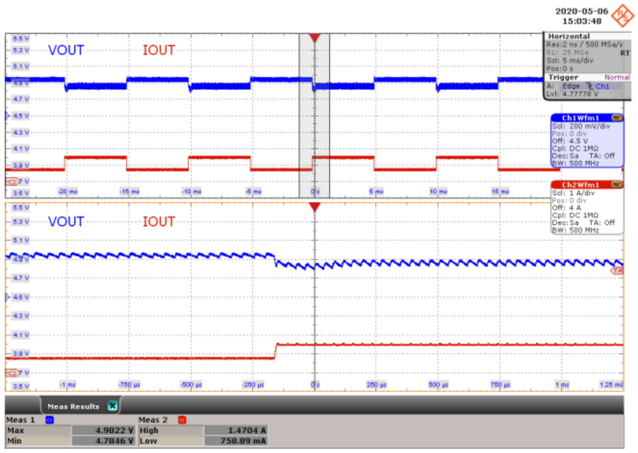

Figure 79 – Transient Response.
90 VAC, 5.0 V, 25% to 50% Load.
V_{OUT} = 4.98 V max, 4.78 V min.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 5 ms / div. (250 µs / div. zoom)

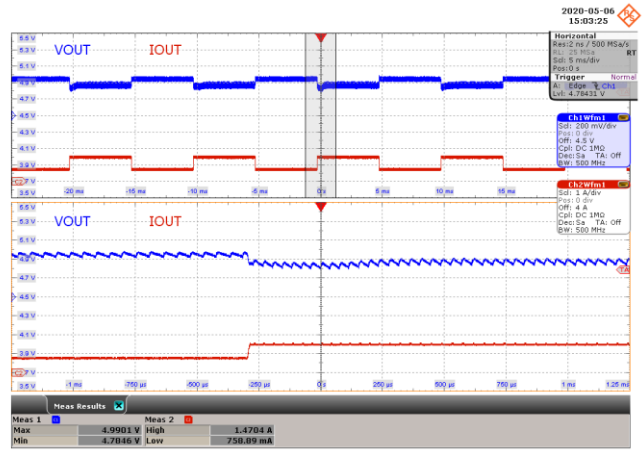

Figure 80 – Transient Response.
265 VAC, 5.0 V, 25% to 50% Load.
V_{OUT} = 4.99 V max, 4.78 V min.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 5 ms / div. (250 µs / div. zoom)

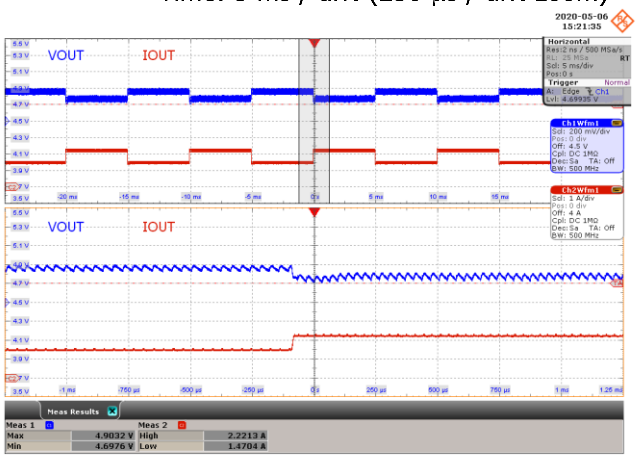

Figure 81 – Transient Response.
90 VAC, 5.0 V, 50% to 75% Load.
V_{OUT} = 4.90 V max, 4.69 V min.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 5 ms / div. (250 µs / div. zoom)

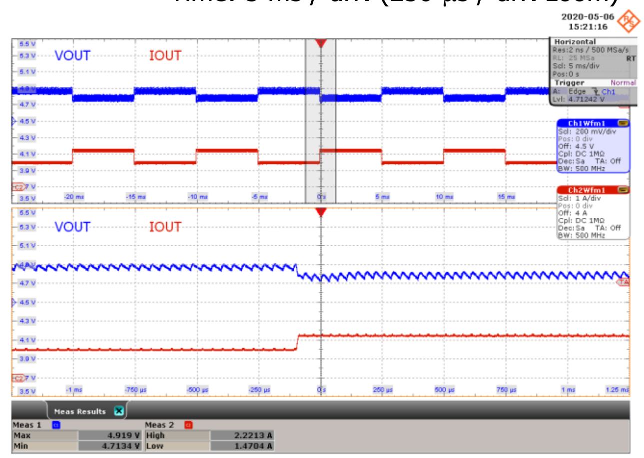

Figure 82 – Transient Response.
265 VAC, 5.0 V, 50% to 75% Load.
V_{OUT} = 4.91 V max, 4.71 V min.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 5 ms / div. (250 µs / div. zoom)

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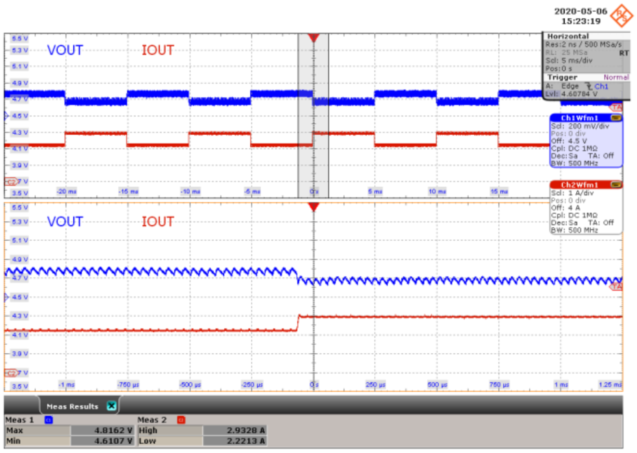

Figure 83 – Transient Response.
90 VAC, 5.0 V, 75% to 100% Load.
V_{OUT} = 4.81 V max, 4.61 V min.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 5 ms / div. (250 µs / div. zoom)

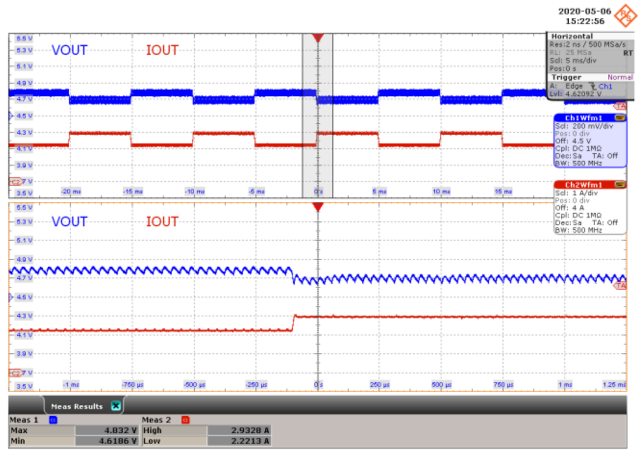

Figure 84 – Transient Response.
265 VAC, 5.0 V, 75% to 100% Load.
V_{OUT} = 4.83 V max, 4.61 V min.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 5 ms / div. (250 µs / div. zoom)

13.6.2 Output: 9 V / 3 A

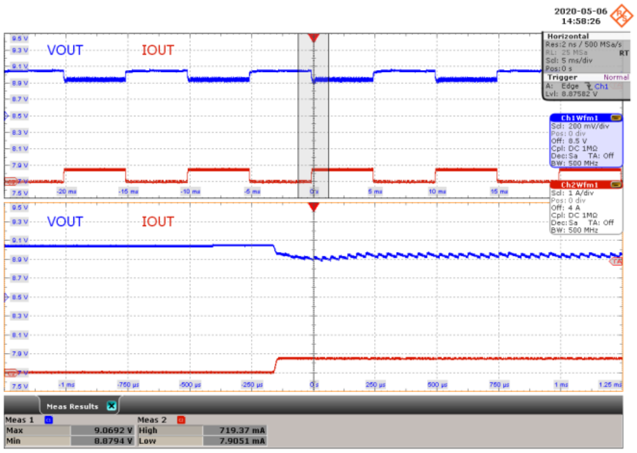

Figure 85 – Transient Response.
90 VAC, 9.0 V, 0 to 25% Load.
V_{OUT} = 9.06 V max, 8.87 V min.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 5 ms / div. (250 µs / div. zoom)

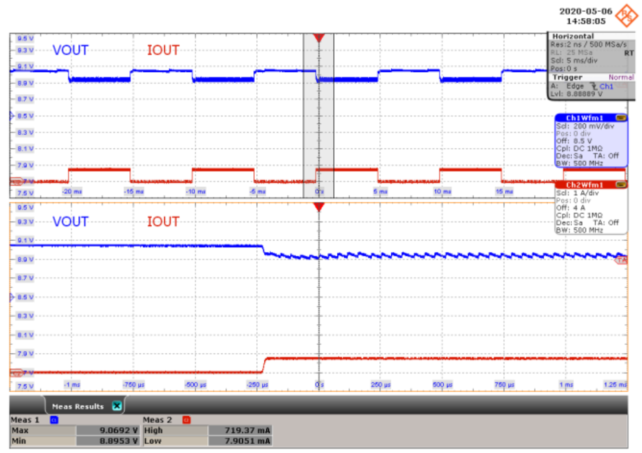

Figure 86 – Transient Response.
265 VAC, 9.0 V, 0 to 25% Load.
V_{OUT} = 9.06 V max, 8.89 V min.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 5 ms / div. (250 µs / div. zoom)

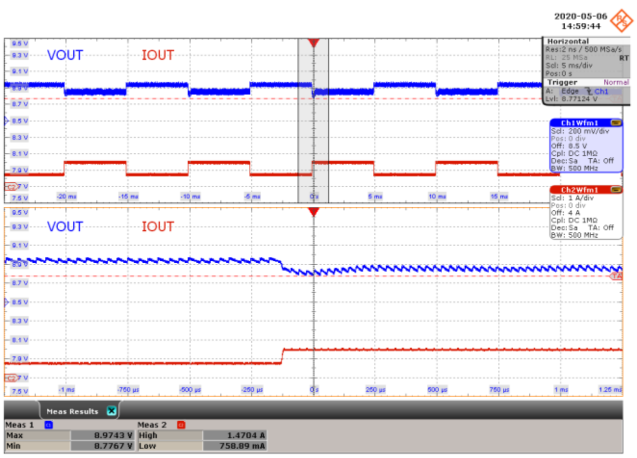

Figure 87 – Transient Response.
90 VAC, 9.0 V, 25% to 50% Load.
V_{OUT} = 8.97 V max, 8.77 V min.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 5 ms / div. (250 µs / div. zoom)

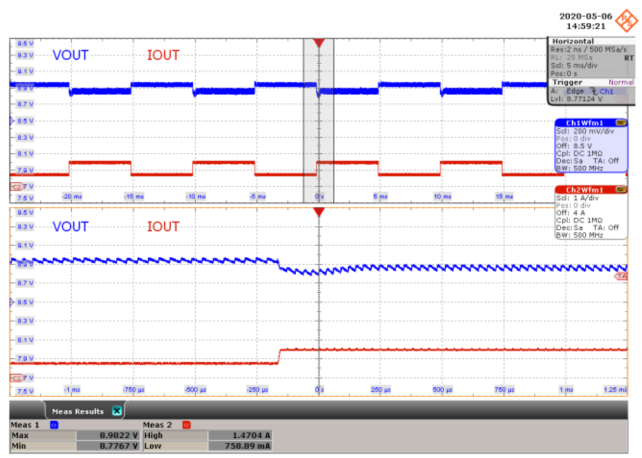

Figure 88 – Transient Response.
265 VAC, 9.0 V, 25% to 50% Load.
V_{OUT} = 8.98 V max, 8.77 V min.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 5 ms / div. (250 µs / div. zoom)

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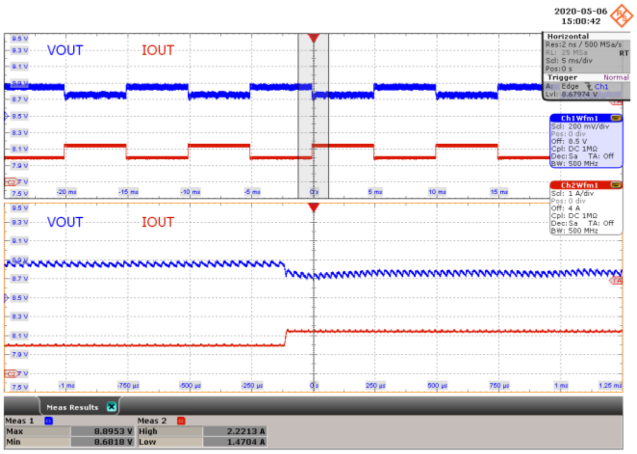

Figure 89 – Transient Response.
90 VAC, 9.0 V, 50% to 75% Load.
V_{OUT} = 8.89 V max, 8.68 V min.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 5 ms / div. (250 µs / div. zoom)

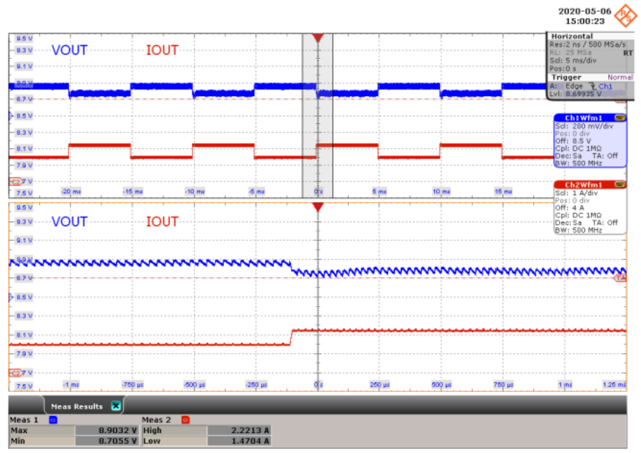

Figure 90 – Transient Response.
265 VAC, 9.0 V, 50% to 75% Load.
V_{OUT} = 8.90 V max, 8.70 V min.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 5 ms / div. (250 µs / div. zoom)

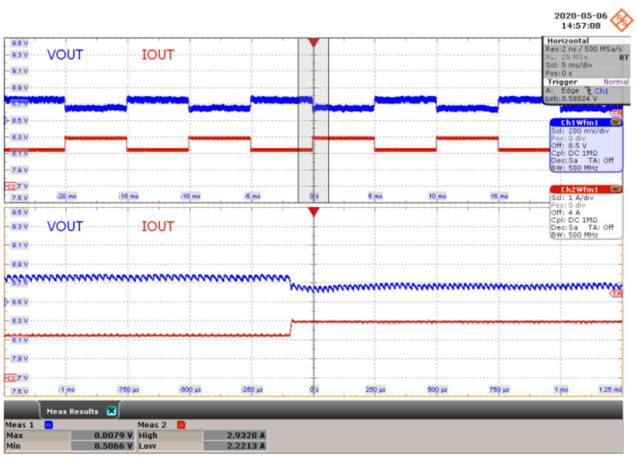

Figure 91 – Transient Response.
90 VAC, 9.0 V, 75% to 100% Load.
V_{OUT} = 8.80 V max, 8.58 V min.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 5 ms / div. (250 µs / div. zoom)

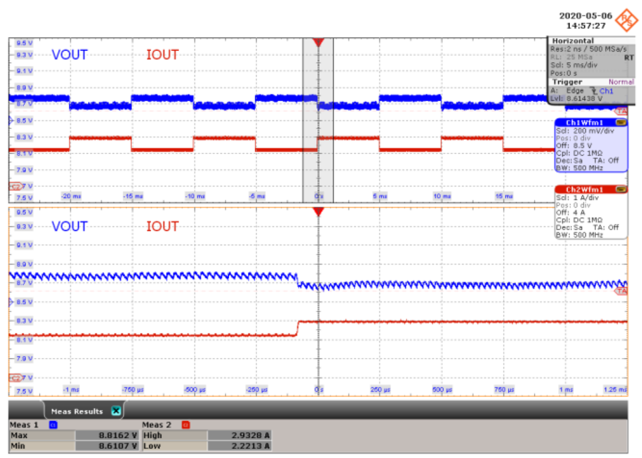

Figure 92 – Transient Response.
265 VAC, 9.0 V, 75% to 100% Load.
V_{OUT} = 8.81 V max, 8.61 V min.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 5 ms / div. (250 µs / div. zoom)

13.6.3 Output: 15 V / 2 A

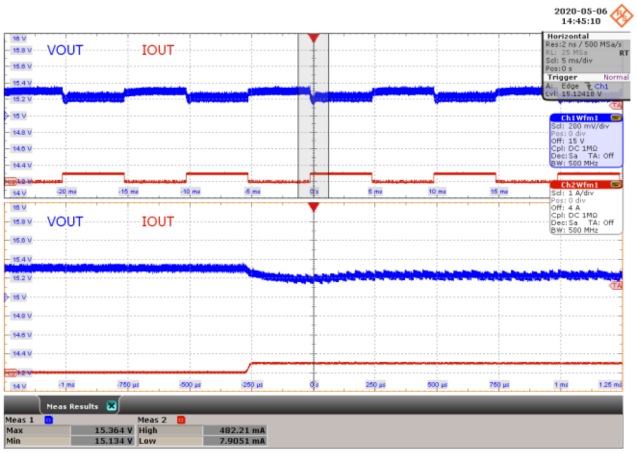

Figure 93 – Transient Response.
90 VAC, 15.0 V, 0 to 25% Load.
V_{OUT} = 15.36 V max, 15.13 V min.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 5 ms / div. (250 µs / div. zoom)

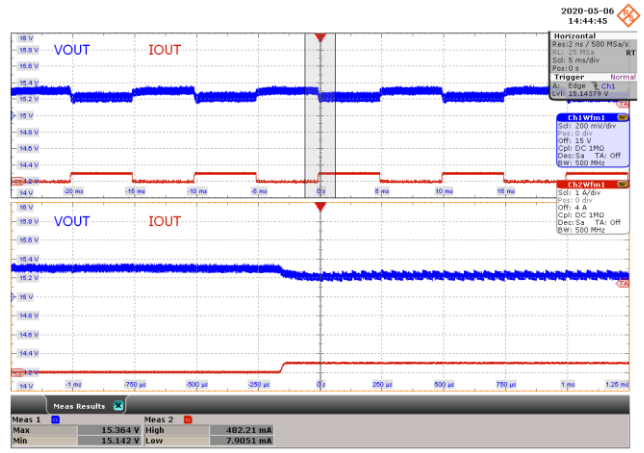

Figure 94 – Transient Response.
265 VAC, 15.0 V, 0 to 25% Load.
V_{OUT} = 15.36 V max, 15.14 V min.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 5 ms / div. (250 µs / div. zoom)

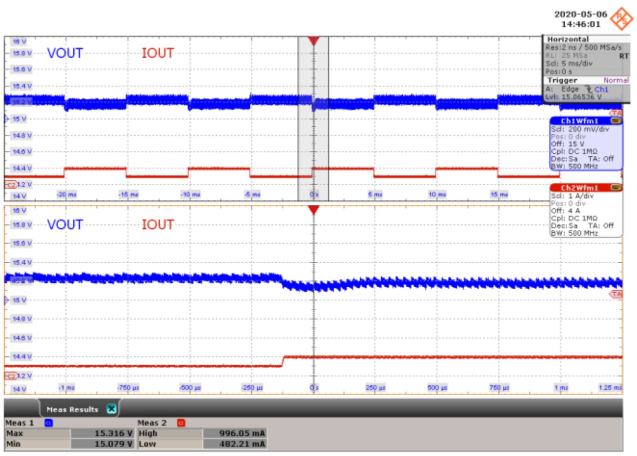

Figure 95 – Transient Response.
90 VAC, 15.0 V, 25% to 50% Load.
V_{OUT} = 15.31 V max, 15.07 V min.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 5 ms / div. (250 µs / div. zoom)

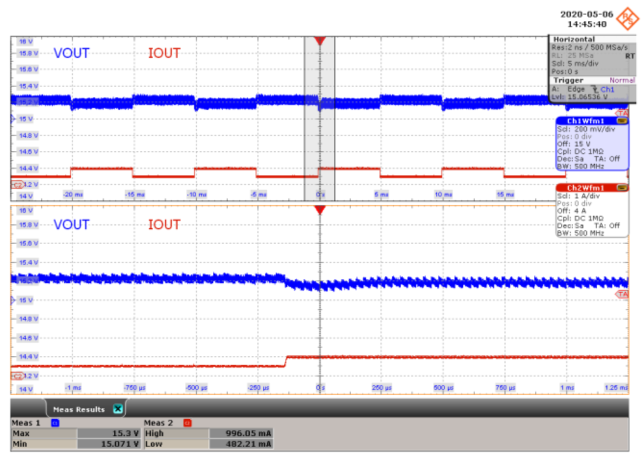

Figure 96 – Transient Response.
265 VAC, 15.0 V, 25% to 50% Load.
V_{OUT} = 15.30 V max, 15.07 V min.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 5 ms / div. (250 µs / div. zoom)

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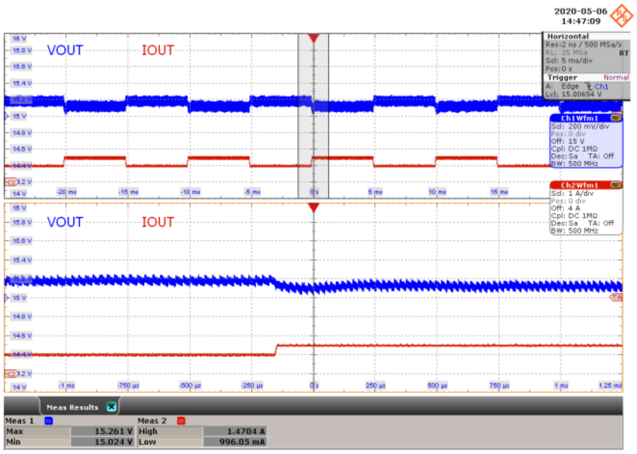

Figure 97 – Transient Response.
90 VAC, 15.0 V, 50% to 75% Load.
V_{OUT} = 15.26 V max, 15.02 V min.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 5 ms / div. (250 µs / div. zoom)

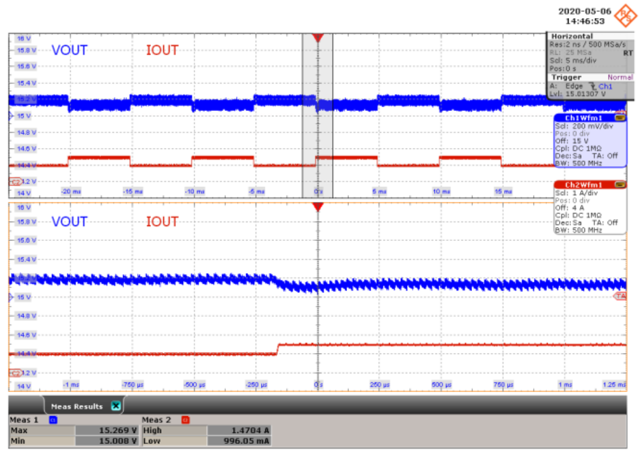

Figure 98 – Transient Response.
265 VAC, 15.0 V, 50% to 75% Load.
V_{OUT} = 15.26 V max, 15.00 V min.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 5 ms / div. (250 µs / div. zoom)

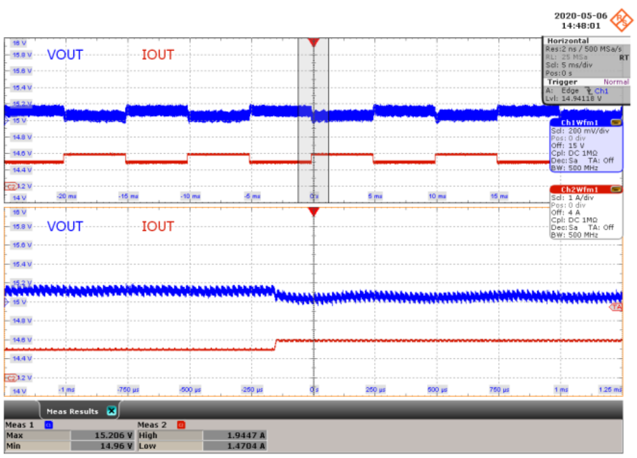

Figure 99 – Transient Response.
90 VAC, 15.0 V, 75% to 100% Load.
V_{OUT} = 15.20 V max, 14.96 V min.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 5 ms / div. (250 µs / div. zoom)

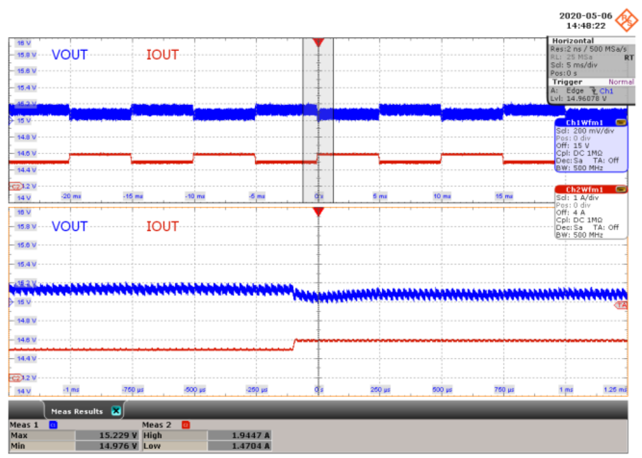

Figure 100 – Transient Response.
265 VAC, 15.0 V, 75% to 100% Load.
V_{OUT} = 15.22 V max, 14.97 V min.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 5 ms / div. (250 µs / div. zoom)

13.6.4 Output: 20 V / 1.5 A

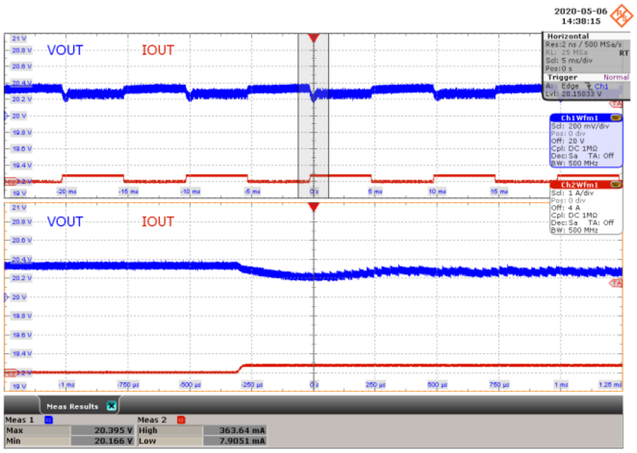

Figure 101 – Transient Response.
90 VAC, 20.0 V, 0 to 25% Load.
V_{OUT} = 20.39 V max, 20.16 V min.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 5 ms / div. (250 µs / div. zoom)

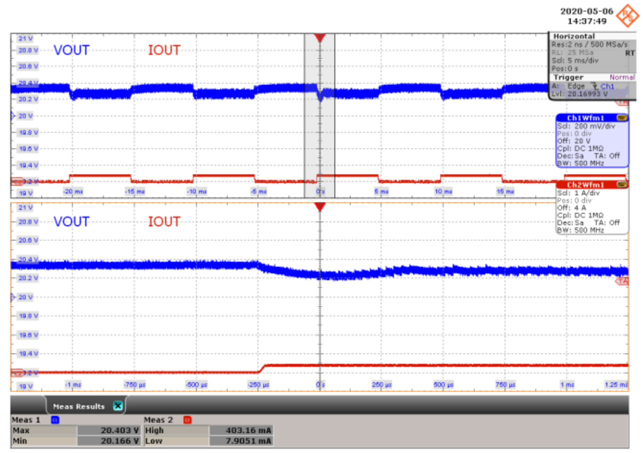

Figure 102 – Transient Response.
265 VAC, 20.0 V, 0 to 25% Load.
V_{OUT} = 20.40 V max, 20.16 V min.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 5 ms / div. (250 µs / div. zoom)

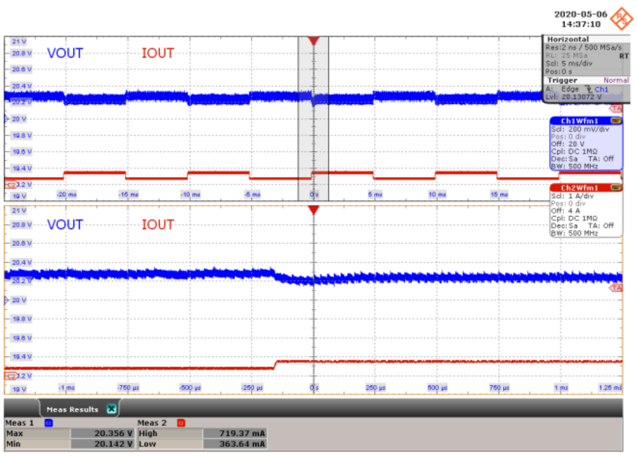

Figure 103 – Transient Response.
90 VAC, 20.0 V, 25% to 50% Load.
V_{OUT} = 20.35 V max, 20.14 V min.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 5 ms / div. (250 µs / div. zoom)

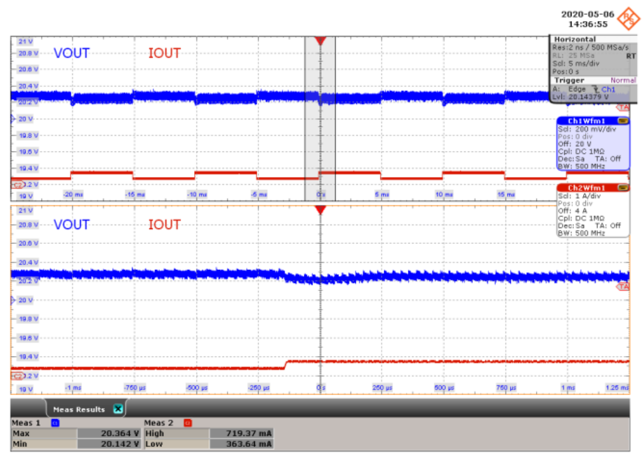

Figure 104 – Transient Response.
265 VAC, 20.0 V, 25% to 50% Load.
V_{OUT} = 20.36 V max, 20.14 V min.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 5 ms / div. (250 µs / div. zoom)

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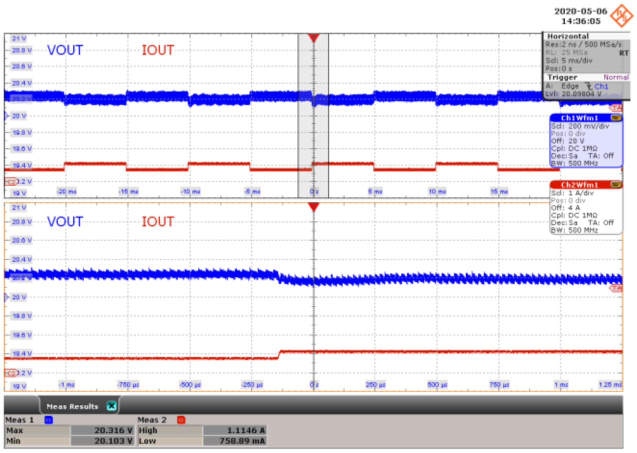

Figure 105 – Transient Response.
90 VAC, 20.0 V, 50% to 75% Load.
V_{OUT} = 20.31 V max, 20.10 V min.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 5 ms / div. (250 µs / div. zoom)

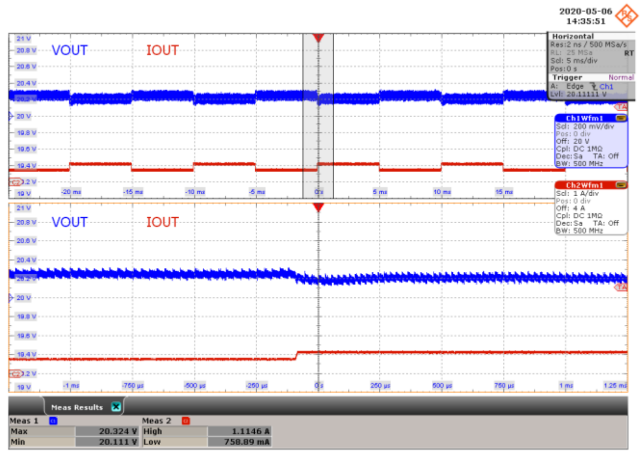

Figure 106 – Transient Response.
265 VAC, 20.0 V, 50% to 75% Load.
V_{OUT} = 20.32 V max, 20.11 V min.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 5 ms / div. (250 µs / div. zoom)

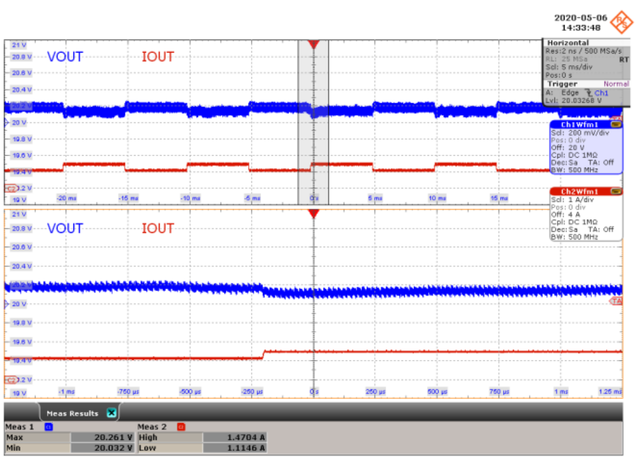

Figure 107 – Transient Response.
90 VAC, 20.0 V, 75% to 100% Load.
V_{OUT} = 20.26 V max, 20.03 V min.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 5 ms / div. (250 µs / div. zoom)

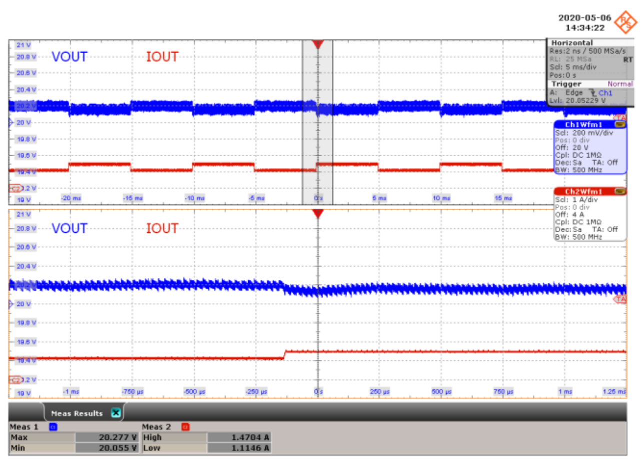

Figure 108 – Transient Response.
265 VAC, 20.0 V, 75% to 100% Load.
V_{OUT} = 20.27 V max, 20.05 V min.
CH1: V_{OUT}, 200 mV / div.
CH2: I_{OUT}, 1 A / div.
Time: 5 ms / div. (250 µs / div. zoom)

13.7 *Output Voltage Ripple Waveforms*

Note: 1. Output voltage waveforms captured at the end of 100 mΩ cable using the ripple measurement probe with decoupling capacitors.

13.7.1 Output: 5 V / 3 A

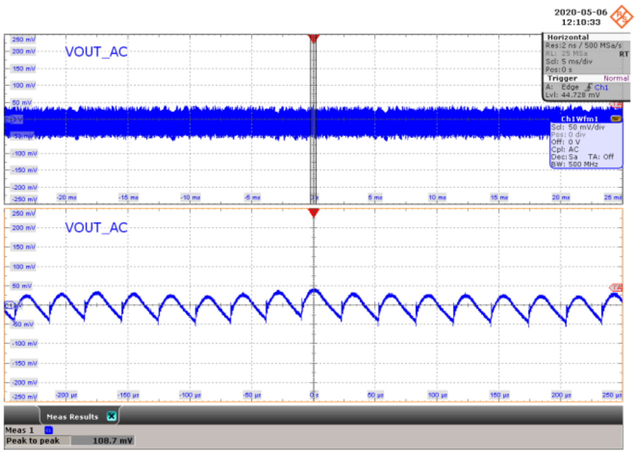

Figure 109 – Output Voltage Ripple.
90 VAC, 5.0 V, 3 A Load.
$V_{OUT(AC)}$ = 108 mV peak-to-peak.
CH1: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (50 µs / div. zoom)

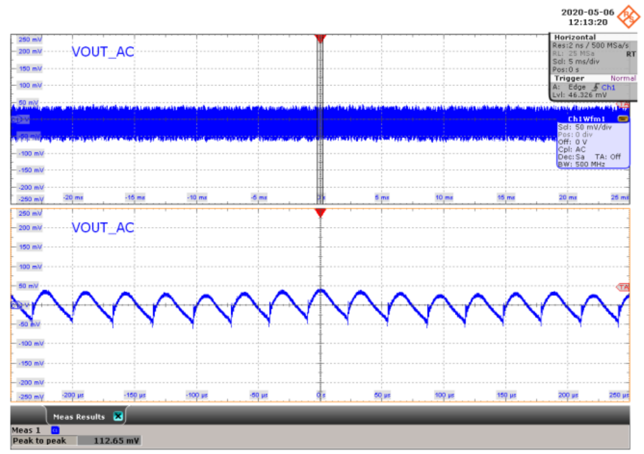

Figure 110 – Output Voltage Ripple.
265 VAC, 5.0 V, 3 A Load.
$V_{OUT(AC)}$ = 112 mV peak-to-peak.
CH1: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (50 µs / div. zoom)

13.7.2 Output: 9 V / 3 A

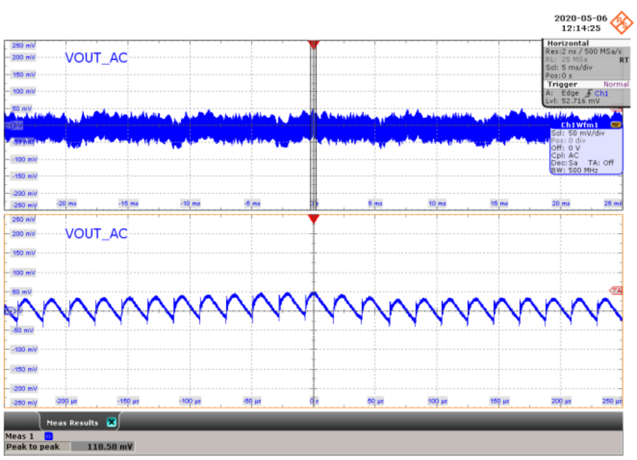

Figure 111 – Output Voltage Ripple.
90 VAC, 9.0 V, 3 A Load.
$V_{OUT(AC)}$ = 118 mV peak-to-peak.
CH1: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (50 µs / div. zoom)

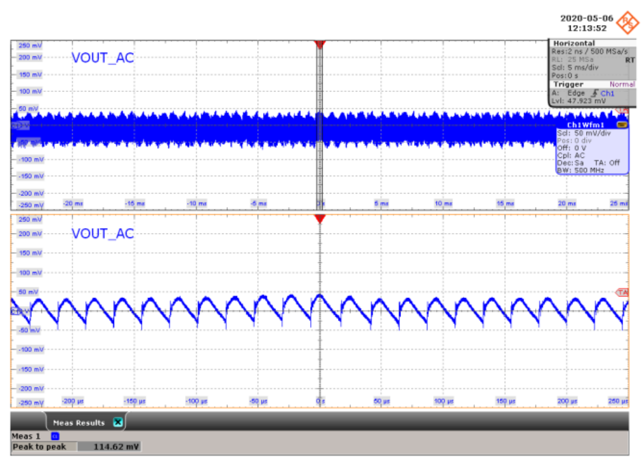

Figure 112 – Output Voltage Ripple.
265 VAC, 9.0 V, 3 A Load.
$V_{OUT(AC)}$ = 114 mV peak-to-peak.
CH1: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (50 µs / div. zoom)

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13.7.3 Output: 15 V / 2 A

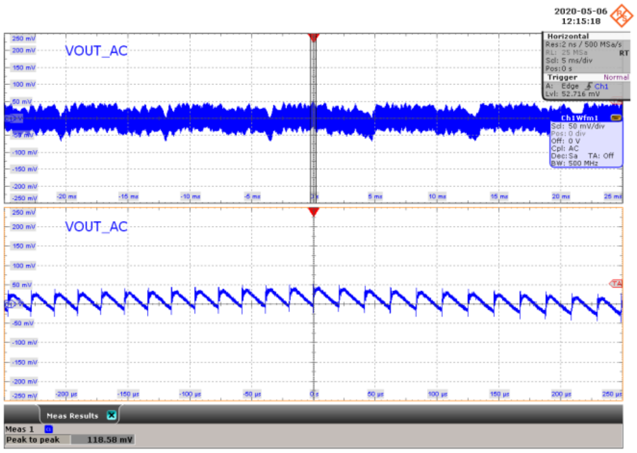

Figure 113 – Output Voltage Ripple.
90 VAC, 15.0 V, 2 A Load.
$V_{OUT(AC)}$ = 118 mV peak-to-peak.
CH1: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (50 µs / div. zoom)

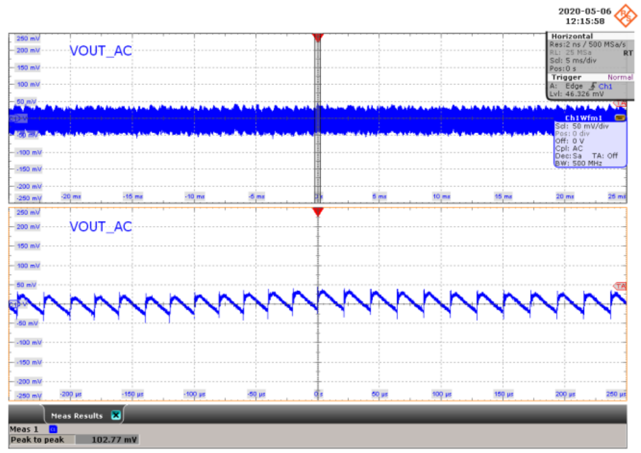

Figure 114 – Output Voltage Ripple.
265 VAC, 15.0 V, 2 A Load.
$V_{OUT(AC)}$ = 102 mV peak-to-peak.
CH1: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (50 µs / div. zoom)

13.7.4 Output: 20 V / 1.5 A

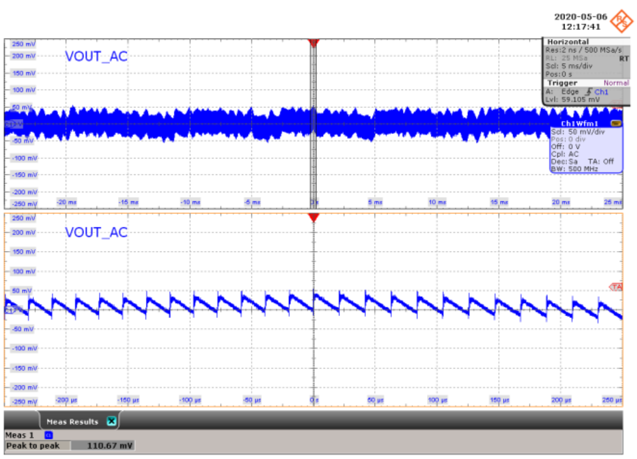

Figure 115 – Output Voltage Ripple.
90 VAC, 20.0 V, 1.5 A Load.
$V_{OUT(AC)}$ = 110 mV peak-to-peak.
CH1: $V_{OUT(AC)}$, 200 mV / div.
Time: 5 ms / div. (50 µs / div. zoom)

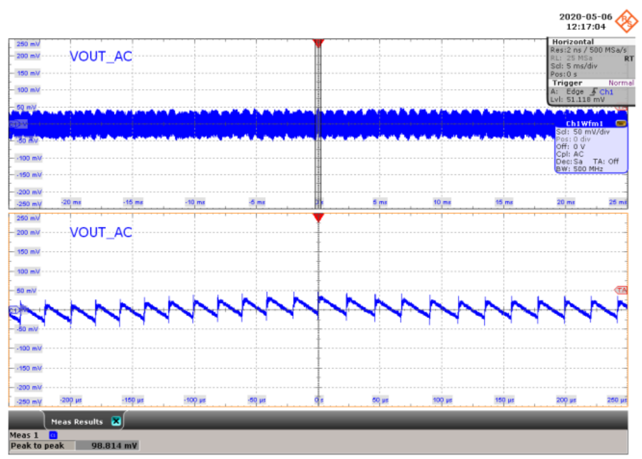

Figure 116 – Output Voltage Ripple.
265 VAC, 20.0 V, 1.5 A Load.
$V_{OUT(AC)}$ = 98 mV peak-to-peak.
CH1: $V_{OUT(AC)}$, 200 mV / div.
Time: 5 ms / div. (50 µs / div. zoom)

13.8 *Output Voltage Ripple Amplitude vs. Load*

13.8.1 Output: 5 V / 3 A

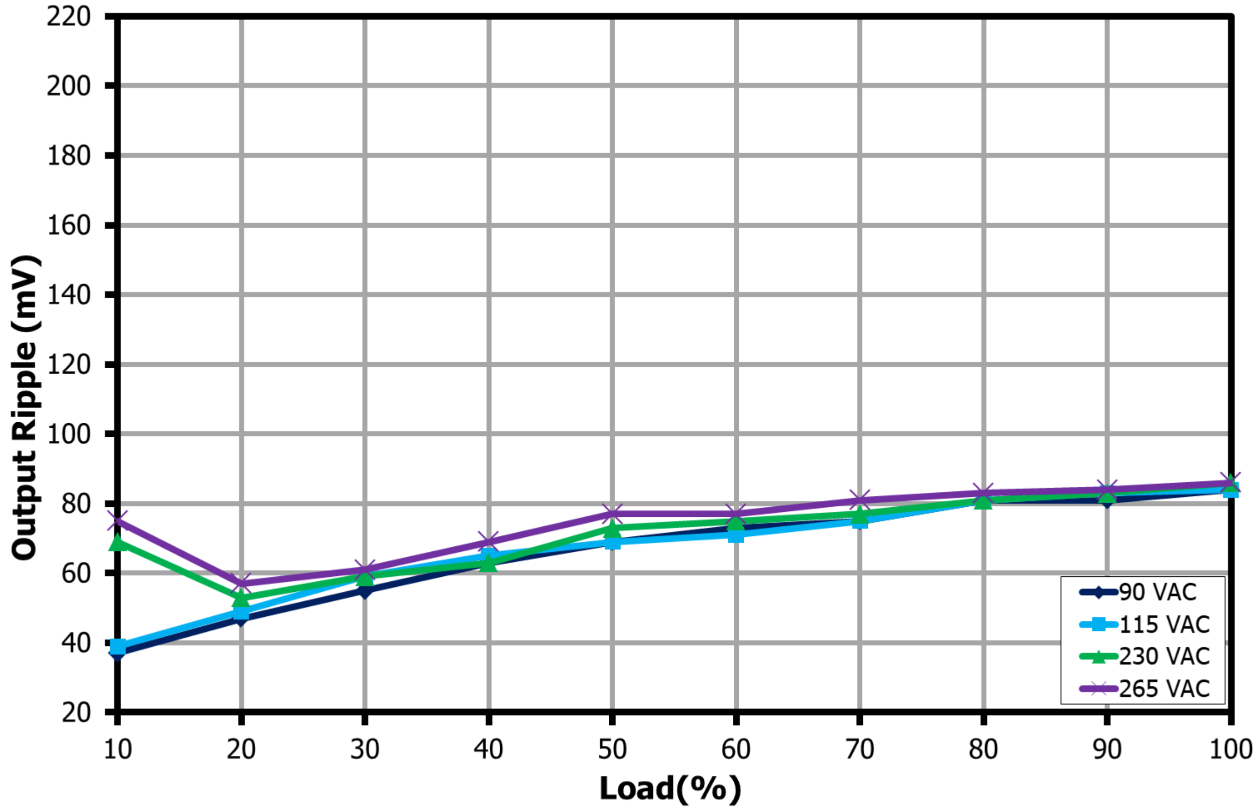

Figure 117 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 5 V Output.

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13.8.2 Output: 9 V / 3 A

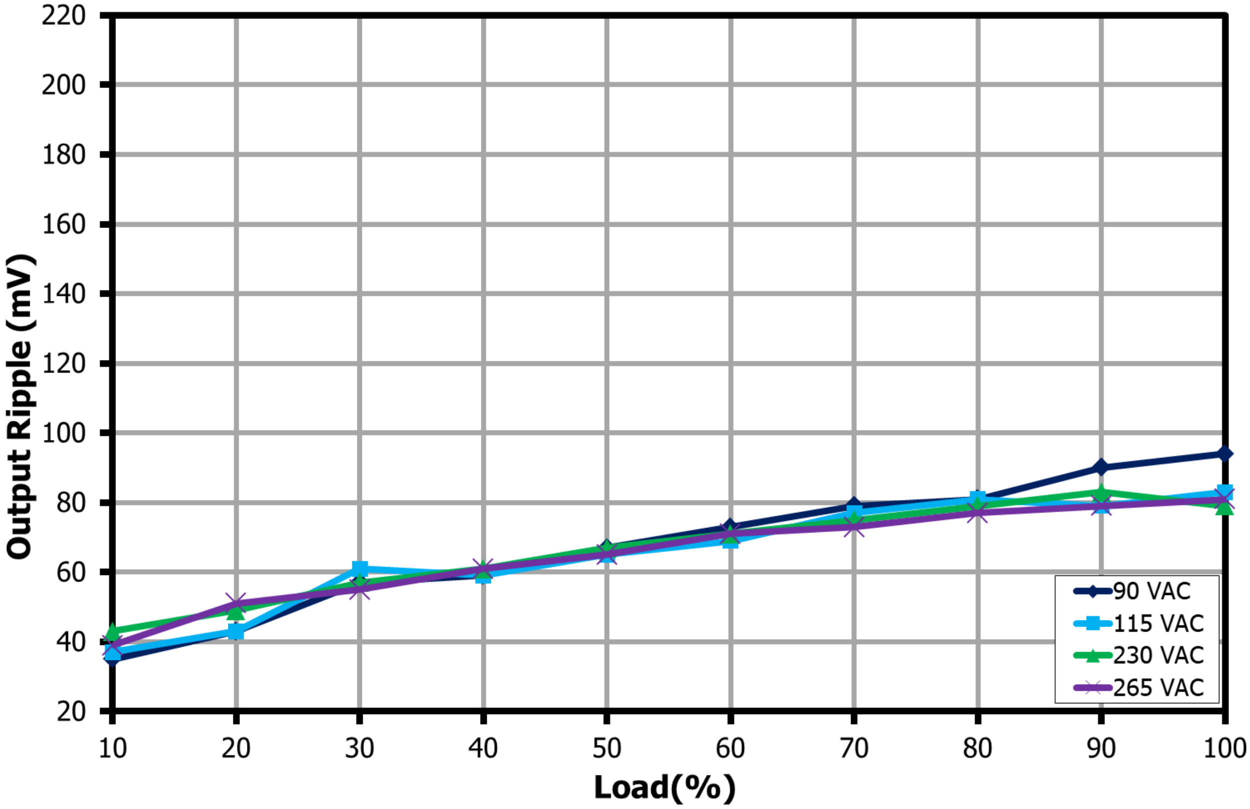

Figure 118 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 9 V Output.

13.8.3 Output: 15 V / 2 A

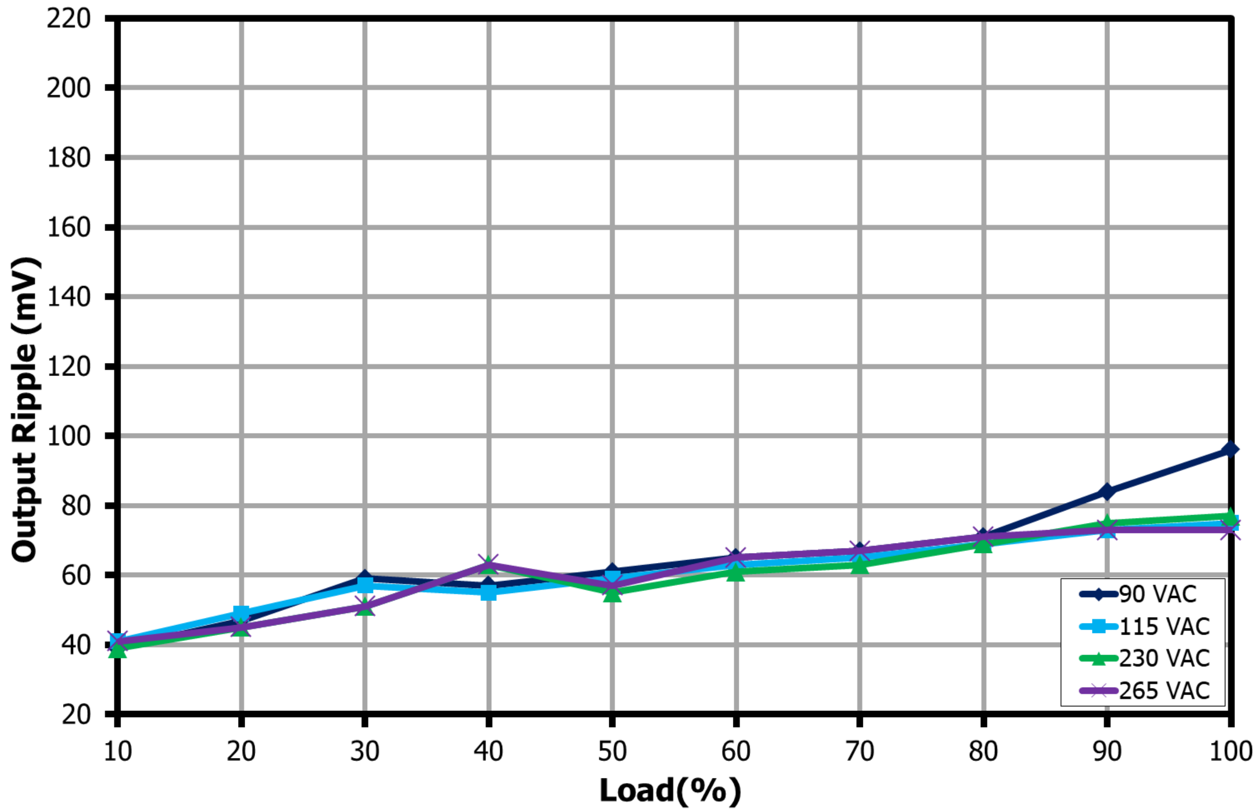

Figure 119 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 15 V Output.

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13.8.4 Output: 20 V / 1.5 A

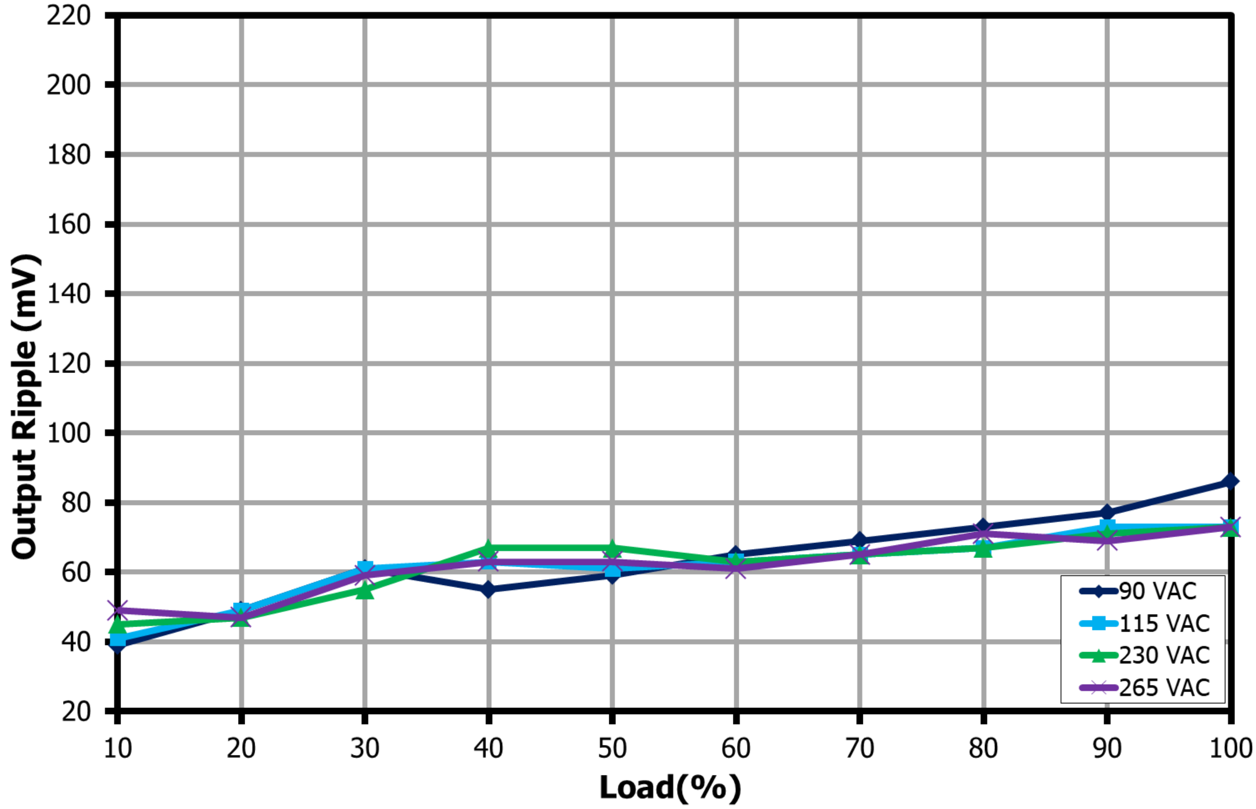

Figure 120 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 20 V Output.

14 CV/CC Profile

Note: 1. Two Programmable Power Supply (PPS) Augmented Power Data Objects (APDO) are supported in this design:

- PDO5: 3.3 V – 11 V / 3 A PPS (30 W power-limited)
- PDO6: 3.3 V – 21 V / 1.5 A PPS (30 W power-limited)

14.1 *Output: 10 V / 3 A PPS Request, PDO5 (30 W Power-Limited)*

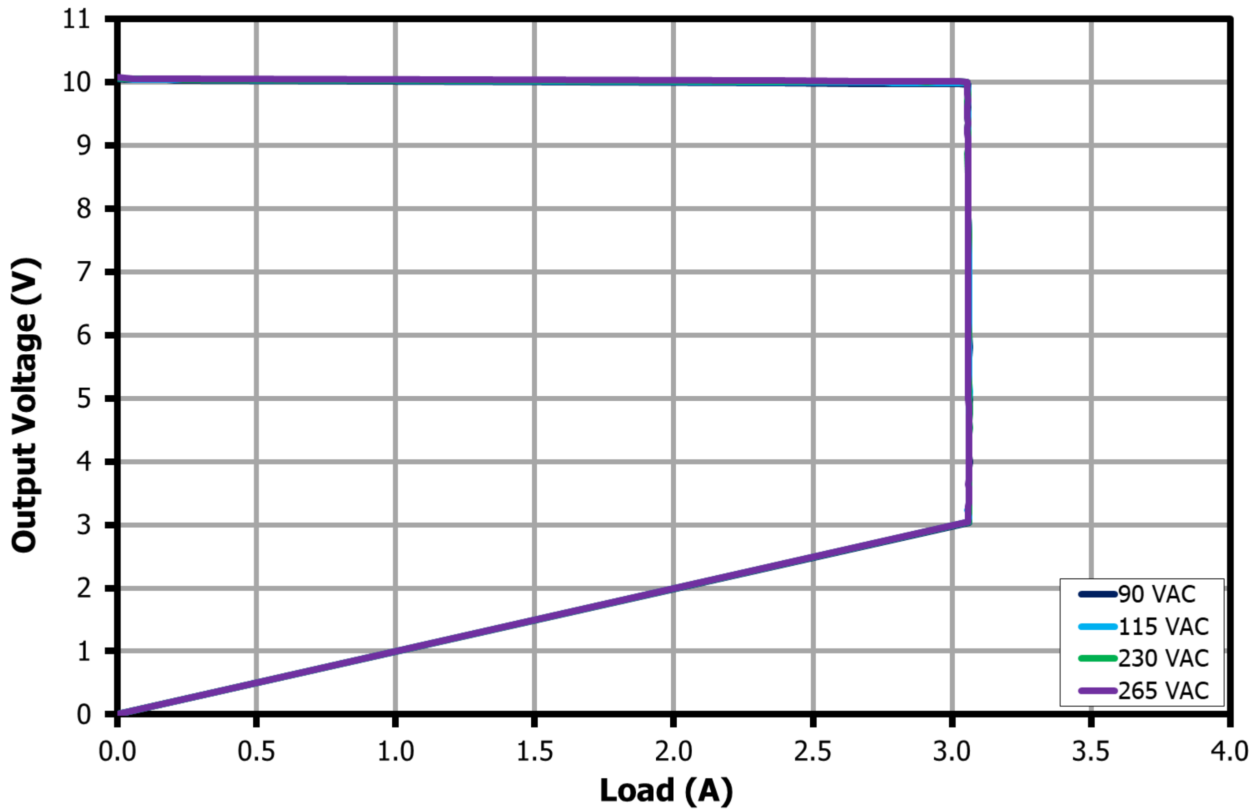

Figure 121 – CV/CC Profile for 10 V / 3 A PPS Request.

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14.2 *Output: 11 V / 3 A PPS Request, PDO5 (30 W Power-Limited)*

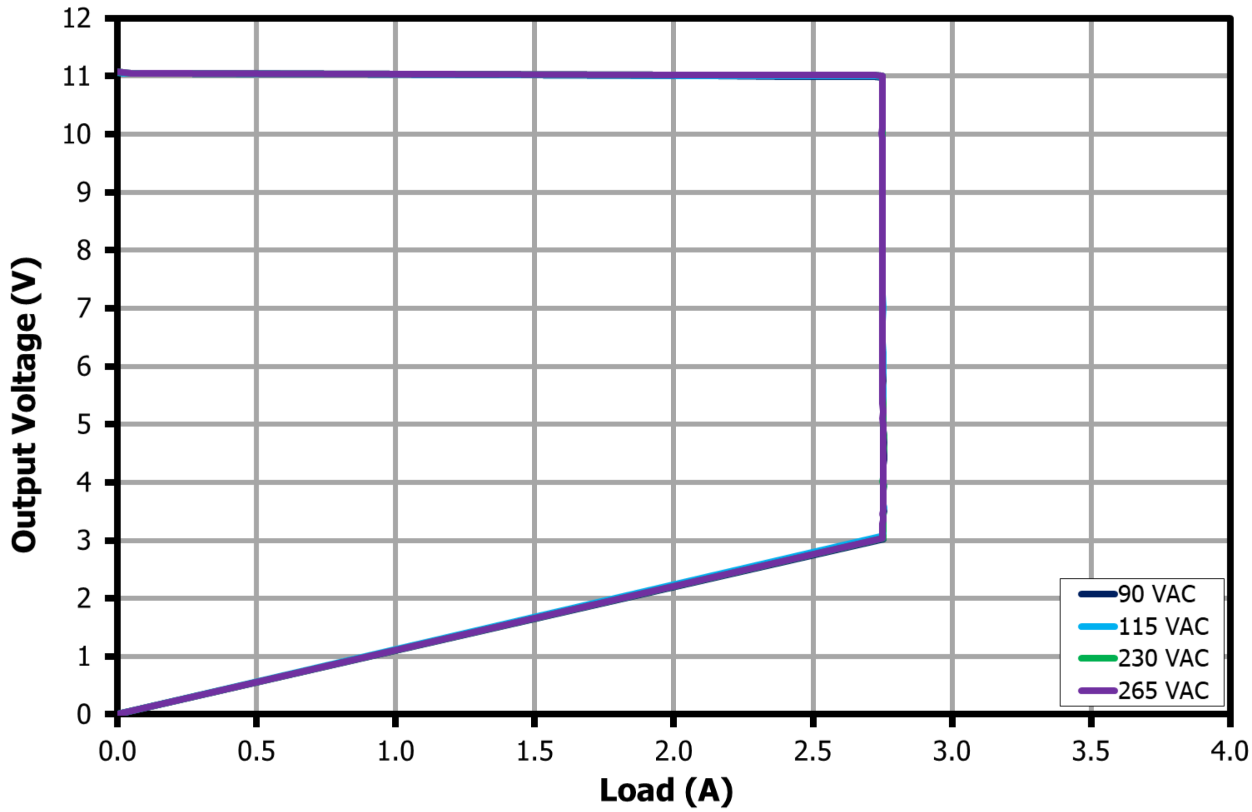

Figure 122 – CV/CC Profile for 11 V / 3 A PPS Request.

14.3 *Output: 20 V / 1.5 A PPS Request, PDO6 (30 W Power-Limited)*

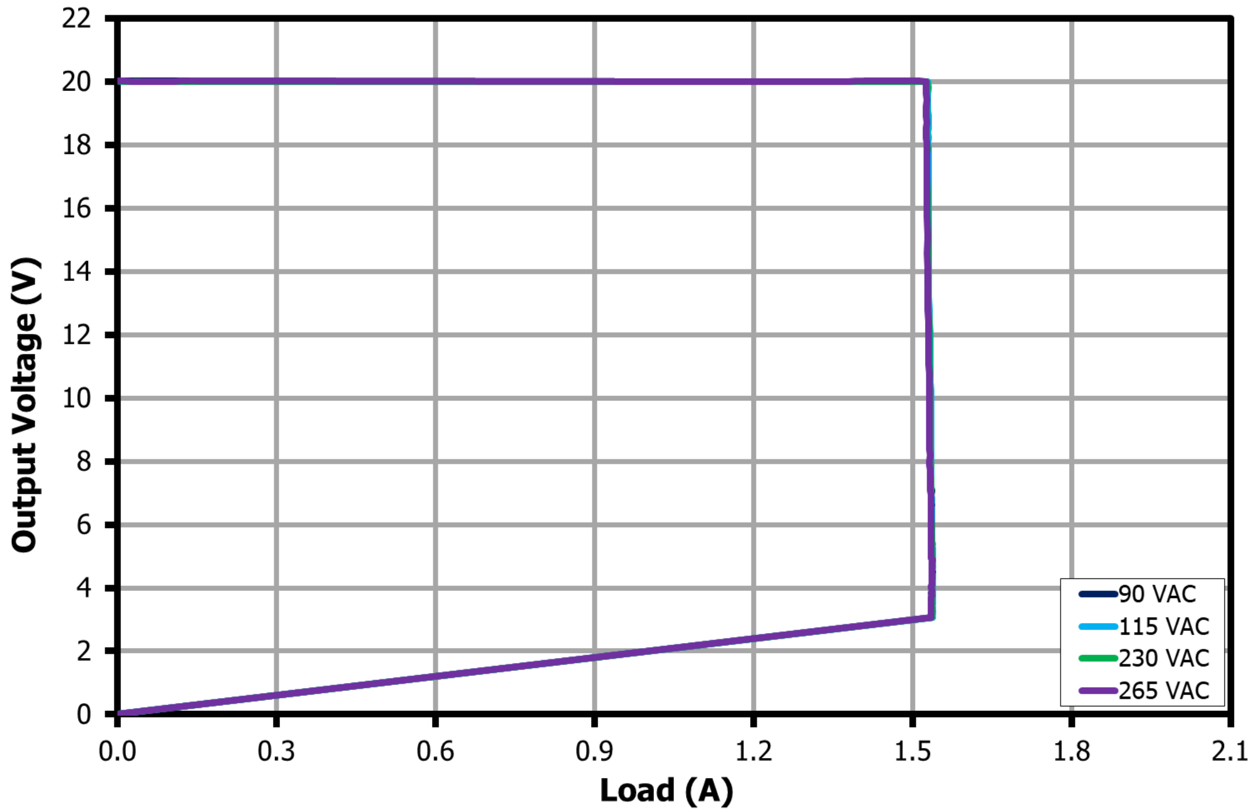

Figure 123 – CV/CC Profile for 20 V / 1.5 A PPS Request.

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14.4 *Output: 21 V / 1.5 A PPS Request, PDO6 (30 W Power-Limited)*

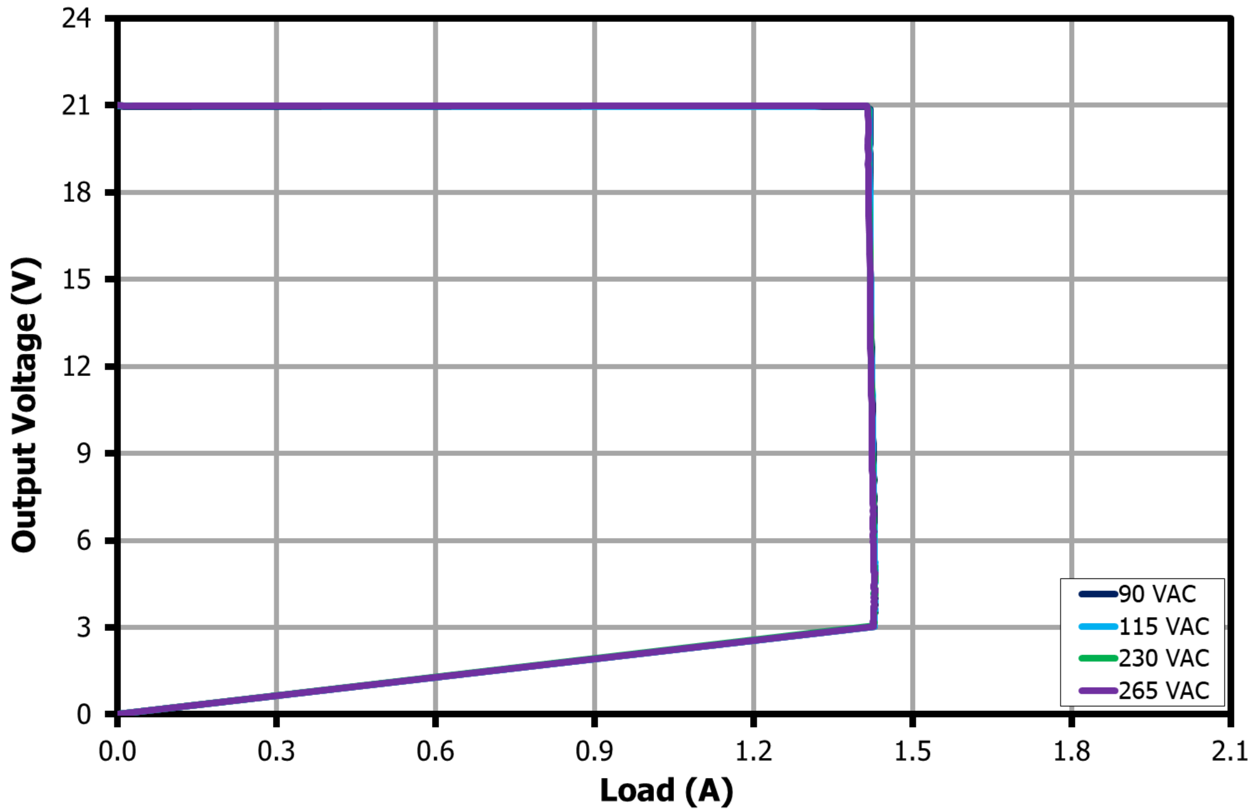

Figure 124 – CV/CC Profile for 21 V / 1.5 A PPS Request.

15 Voltage Step and Current Limit Test using Quadramax and Total Phase Analyzer

15.1 *Voltage Step Test (VST)*

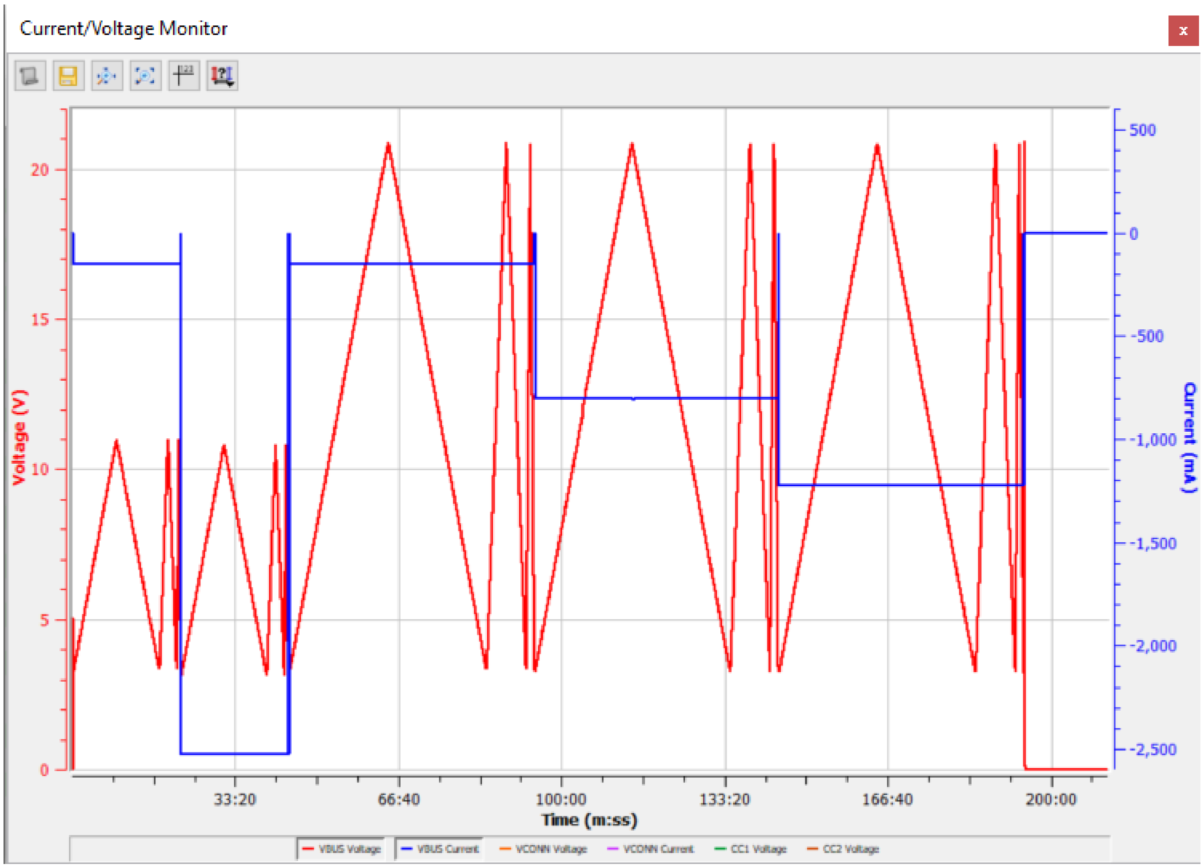

Figure 125 – Plot of SPT.6 VST from Total Phase Analyzer.

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15.2 *Current Limit Test (CLT)*

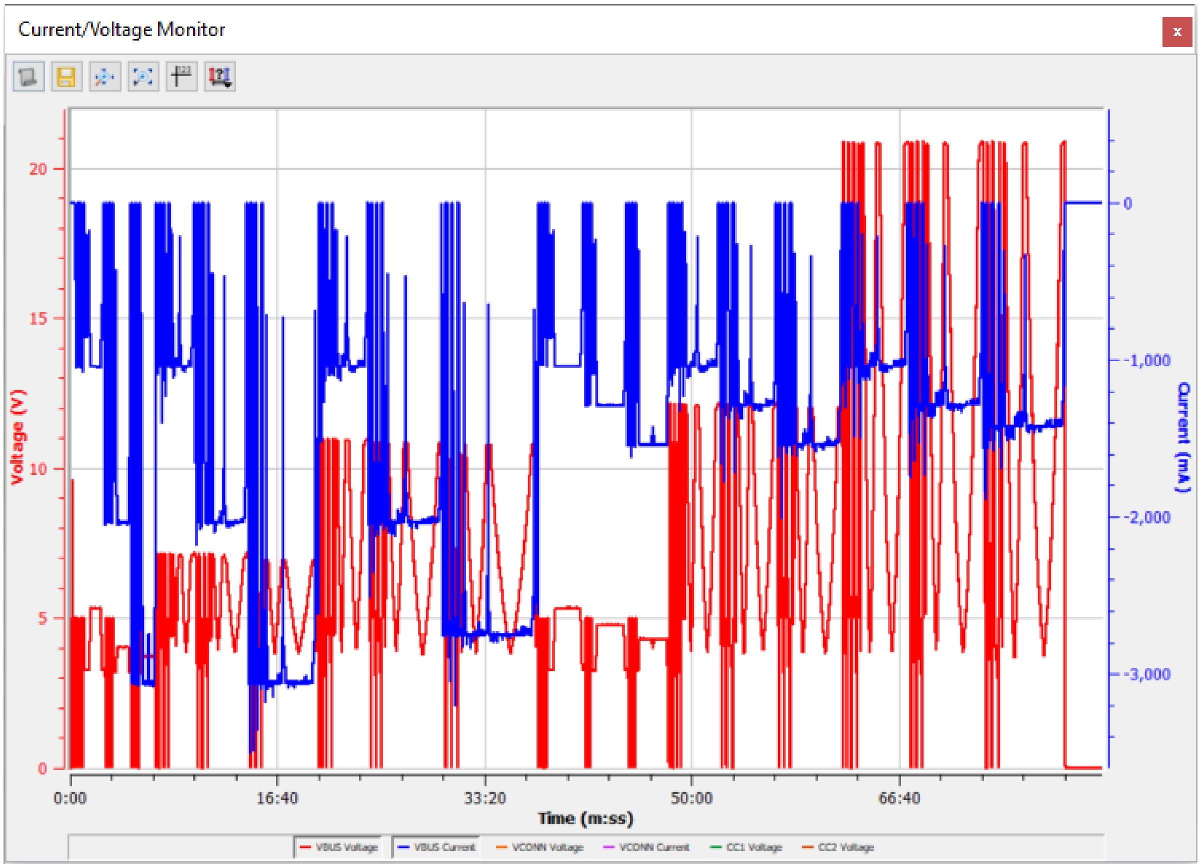
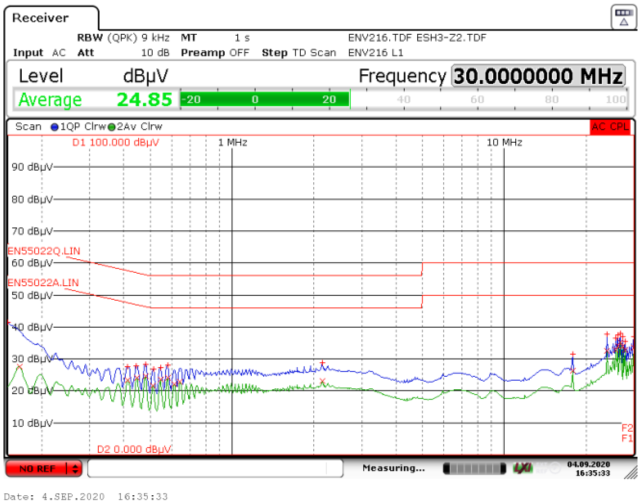


Figure 126 – Plot of SPT.7 CLT from Total Phase Analyzer.

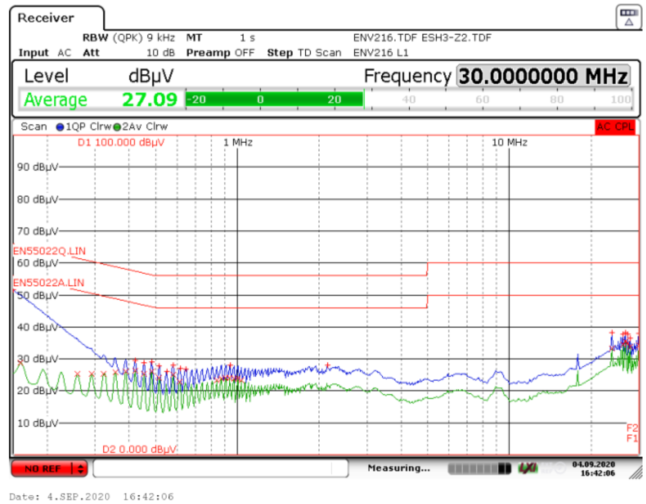
16 Conducted EMI

16.1 *Floating Ground (QPK / AV)*

16.1.1 Output: 5 V / 3 A

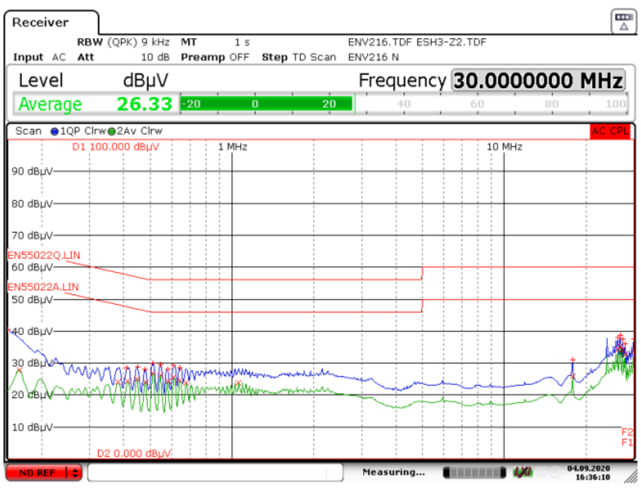


115 VAC.

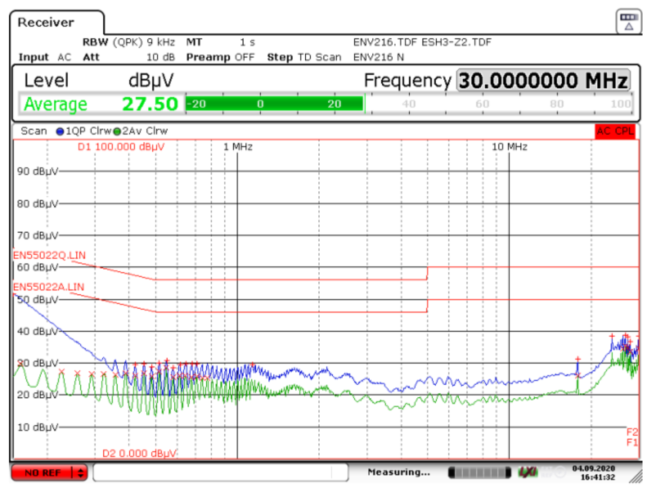


230 VAC.

Figure 127 – Floating Ground EMI, 5 V / 3 A Load [Line Scan].



115 VAC.



230 VAC.

Figure 128 – Floating Ground EMI, 5 V / 3 A Load [Neutral Scan].

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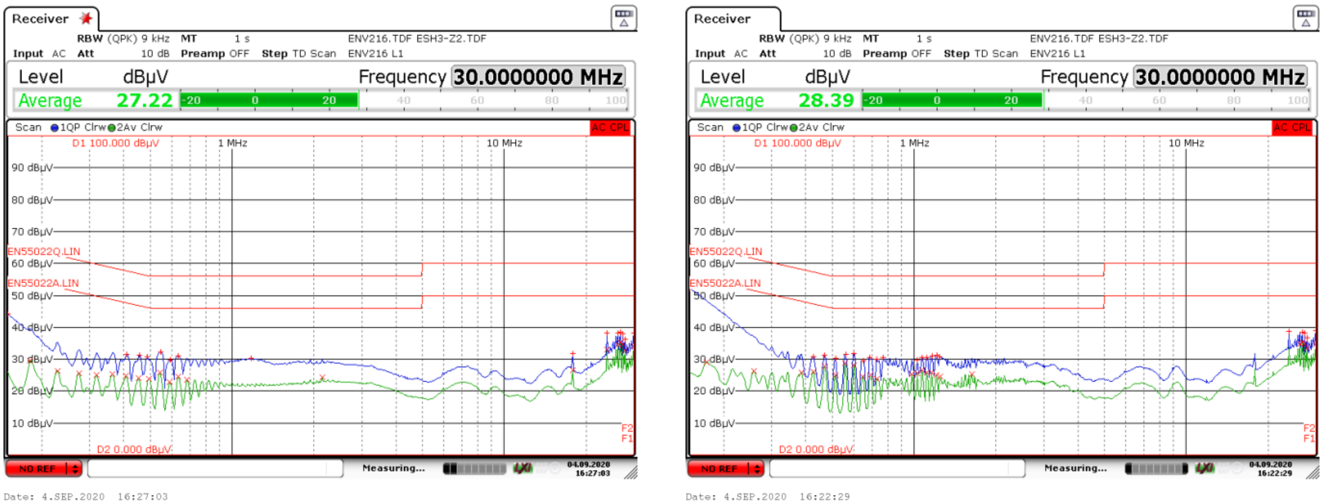
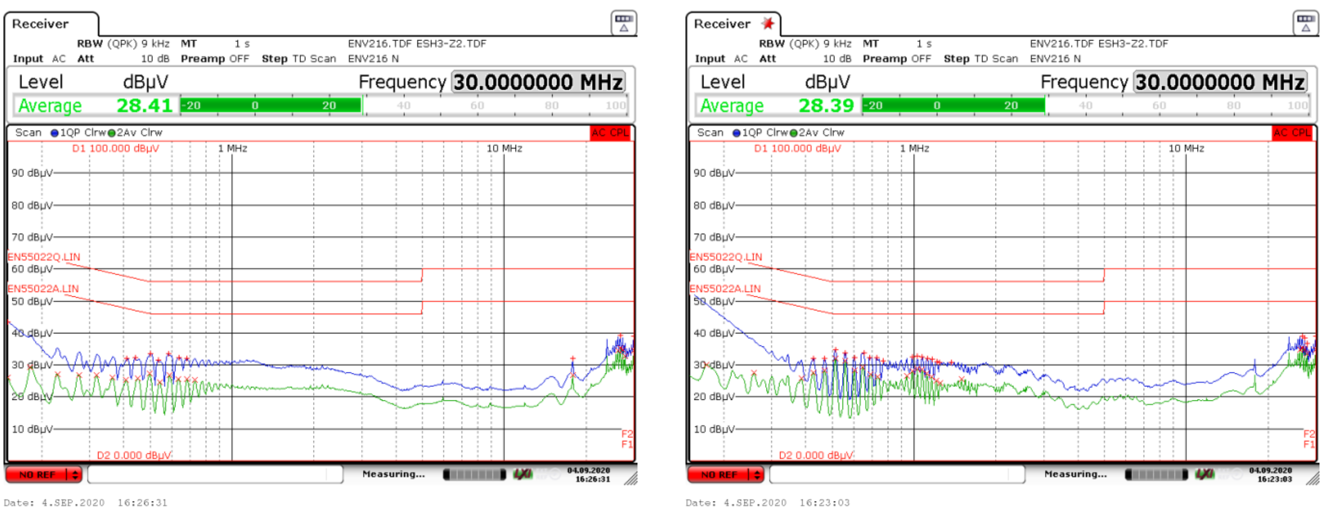
16.1.2 Output: 9 V / 3 A



115 VAC. 230 VAC.

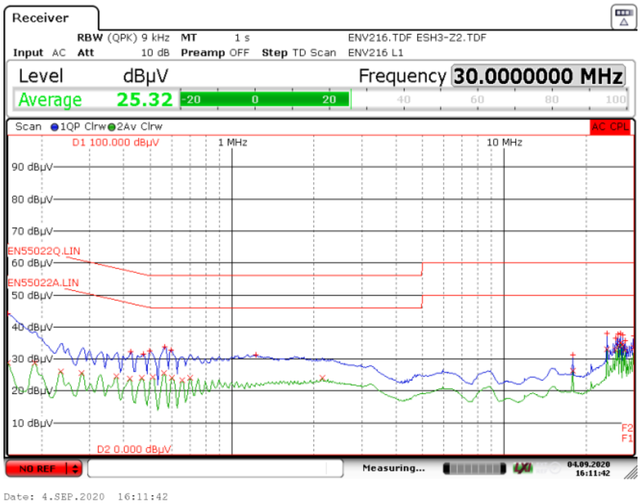
Figure 129 – Floating Ground EMI, 9 V / 3 A Load [Line Scan].

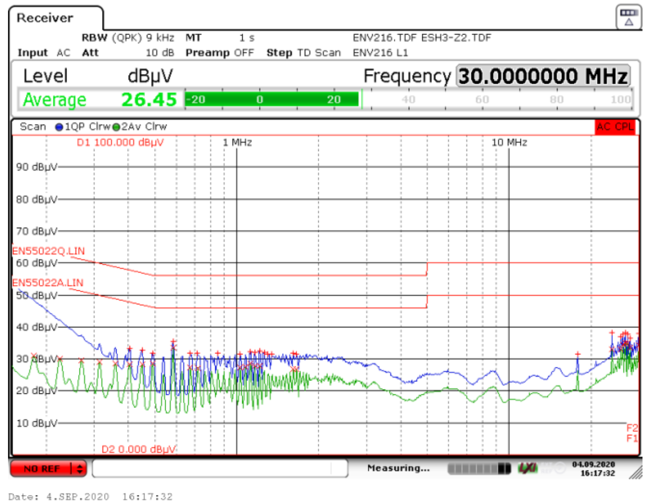


115 VAC. 230 VAC.

Figure 130 – Floating Ground EMI, 9 V / 3 A Load [Neutral Scan].

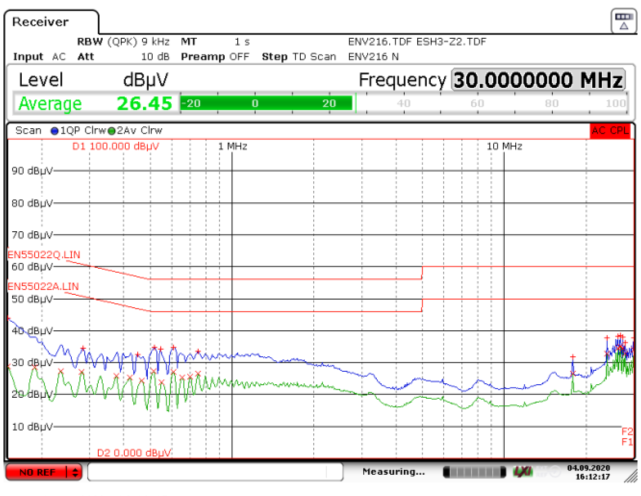
16.1.3 Output: 15 V / 2 A

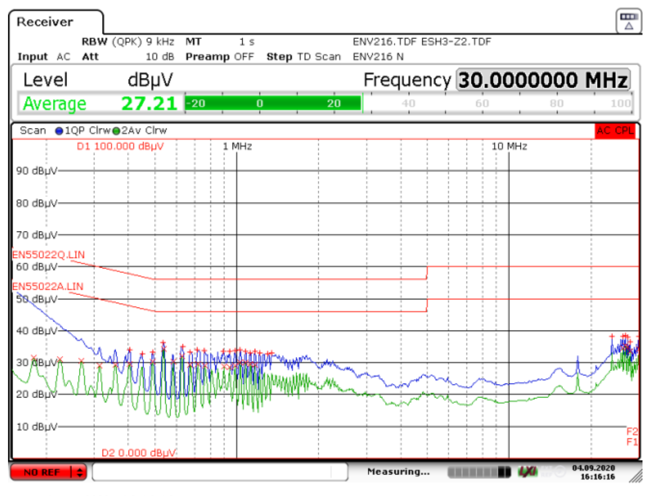




115 VAC. 230 VAC.

Figure 131 – Floating Ground EMI, 15 V / 2 A Load [Line Scan].





115 VAC. 230 VAC.

Figure 132 – Floating Ground EMI, 15 V / 2 A Load [Neutral Scan].

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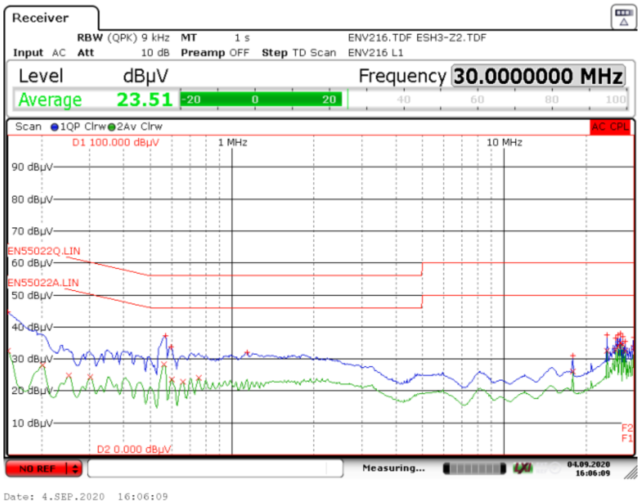
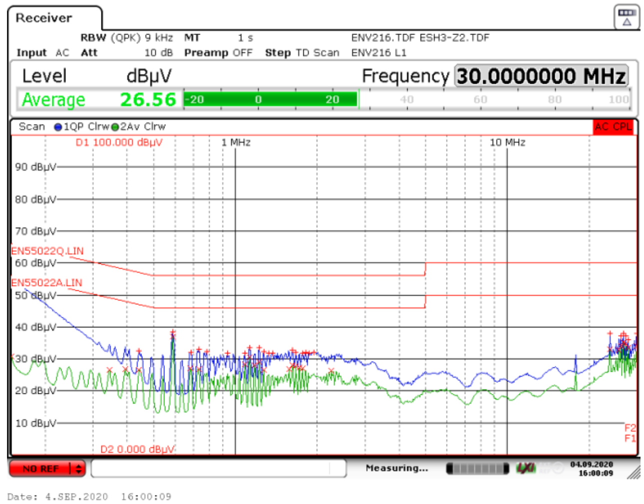
16.1.4 Output: 20 V / 1.5 A

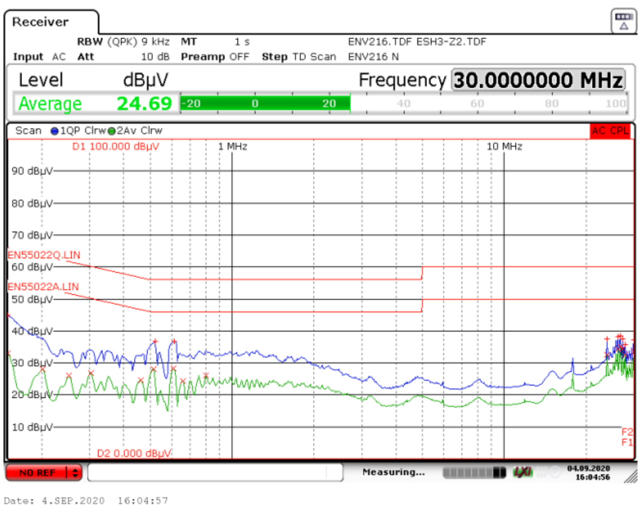


115 VAC.

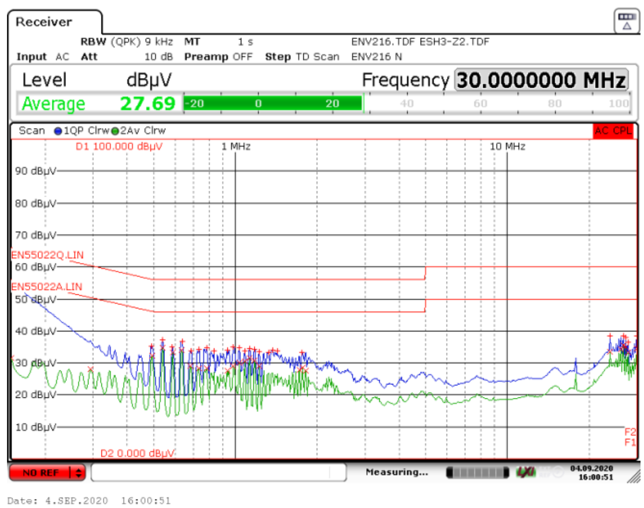


230 VAC.

Figure 133 – Floating Ground EMI, 20 V / 1.5 A Load [Line Scan].



115 VAC.



230 VAC.

Figure 134 – Floating Ground EMI, 20 V / 1.5 A Load [Neutral Scan].

17 Combination Wave Surge

The unit was subjected to ±1500 V differential mode and ±2000 V common mode combination wave surge at several line phase angles with 10 strikes for each condition.

A test failure was defined as an output latch-off that needs operator intervention to recover, or a complete loss of function that is not recoverable.

17.1 *Differential Mode Surge (L1 to L2), 230 VAC Input*

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 5 V / 0 A	Test Result 20 V / 1.5 A
+1500	L1 to L2	0	Pass	Pass
-1500	L1 to L2	0	Pass	Pass
+1500	L1 to L2	90	Pass[1]	Pass[1]
-1500	L1 to L2	90	Pass	Pass
+1500	L1 to L2	270	Pass	Pass
-1500	L1 to L2	270	Pass[1]	Pass[1]

[1]Power supply might initiate Auto-Restart protection due to Line OV condition

17.2 *Common Mode Surge (L1, L2 to PE), 230 VAC Input*

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 5 V / 0 A	Test Result 20 V / 1.5 A
+2000	L1, L2 to PE	0	Pass	Pass
-2000	L1, L2 to PE	0	Pass	Pass
+2000	L1, L2 to PE	90	Pass	Pass
-2000	L1, L2 to PE	90	Pass	Pass
+2000	L1, L2 to PE	270	Pass	Pass
-2000	L1, L2 to PE	270	Pass	Pass

17.3 *Common Mode Surge (L1 to PE), 230 VAC Input*

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 5 V / 0 A	Test Result 20 V / 1.5 A
+2000	L1 to PE	0	Pass	Pass
-2000	L1 to PE	0	Pass	Pass
+2000	L1 to PE	90	Pass	Pass
-2000	L1 to PE	90	Pass[1]	Pass[1]
+2000	L1 to PE	270	Pass[1]	Pass[1]
-2000	L1 to PE	270	Pass	Pass

[1]Power supply might initiate Auto-Restart protection due to Line OV condition.

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17.4 *Common Mode Surge (L2 to PE), 230 VAC Input*

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 5 V / 0 A	Test Result 20 V / 1.5 A
+2000	L2 to PE	0	Pass	Pass
-2000	L2 to PE	0	Pass	Pass
+2000	L2 to PE	90	Pass[1]	Pass[1]
-2000	L2 to PE	90	Pass	Pass
+2000	L2 to PE	270	Pass	Pass
-2000	L2 to PE	270	Pass[1]	Pass[1]

[1]Power supply might initiate Auto-Restart protection due to Line OV condition

Note: Surge events might trigger input line OV Protection and initiate an auto-restart. Auto-restart (AR) is one of the safety features of InnoSwitch3-Pro to protect the converter from fault conditions. For applications that require completely no output interruption, the design can be modified to have a higher input line OVP voltage threshold or with the input line OVP completely disabled.

18 Electrostatic Discharge

The unit was tested with ±8 kV to ±16.5 kV air discharge and ±8.8 kV contact discharge with 10 strikes for each condition at the following locations:

- End of cable +VOUT
- End of cable GND
- On-board +VOUT
- On-board GND
- End of cable CC1
- End of cable CC2

A test failure was defined as an output latch-off that needs operator intervention to recover, or a complete loss of function that is not recoverable.

Note: 1. Fish paper insulator (10 mil thick) is inserted into the PCB slot for ESD tests
2. End of cable discharge points (VOUT, GND, CC1, CC2) located on the USB-C power adapter tester Tiny-PAT
3. Type-C cable for all test conditions: Passive 3 A cable, 1 meter (Google)

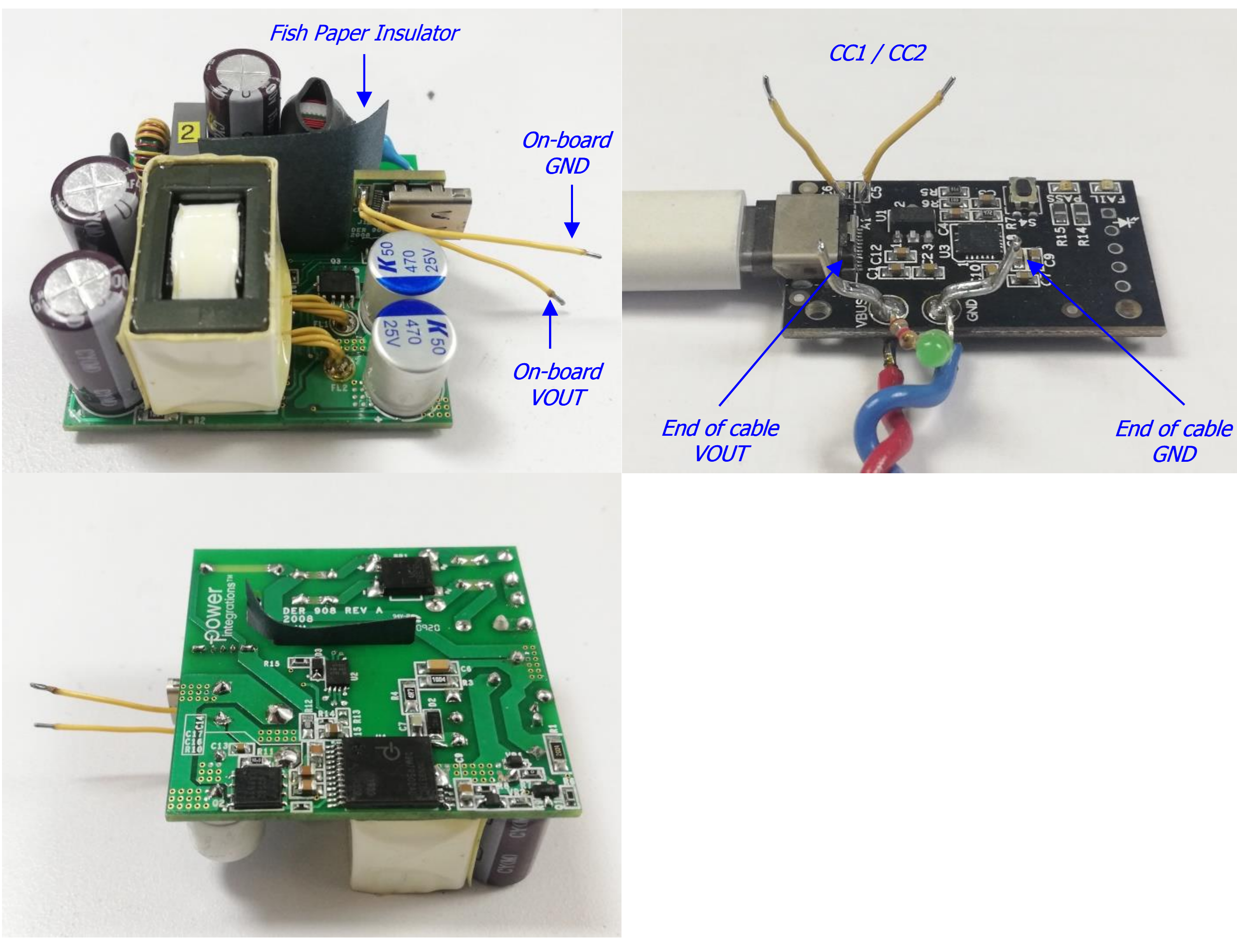

Figure 135 – Fish Paper Insulator and ESD Discharge Points.

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18.1 *Air Discharge, +VOUT and GND, 230 VAC Input*

Discharge Voltage (kV)	ESD Strike Location		Test Result 5 V / 0 A	Test Result 20 V / 1.5 A
+8	End of Cable	+VOUT	Pass	Pass
		GND	Pass	Pass
-8		+VOUT	Pass	Pass
		GND	Pass	Pass
+10		+VOUT	Pass	Pass
		GND	Pass	Pass
-10		+VOUT	Pass	Pass
		GND	Pass	Pass
+12		+VOUT	Pass	Pass
		GND	Pass	Pass
-12		+VOUT	Pass	Pass
		GND	Pass	Pass
+14		+VOUT	Pass	Pass
		GND	Pass	Pass
-14		+VOUT	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]
+16.5		+VOUT	Pass	Pass
		GND	Pass	Pass
-16.5		+VOUT	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]
+8	On the Board	+VOUT	Pass	Pass
		GND	Pass	Pass
-8		+VOUT	Pass	Pass
		GND	Pass	Pass
+10		+VOUT	Pass	Pass
		GND	Pass	Pass
-10		+VOUT	Pass	Pass
		GND	Pass	Pass
+12		+VOUT	Pass	Pass
		GND	Pass	Pass
-12		+VOUT	Pass	Pass
		GND	Pass	Pass
+14		+VOUT	Pass	Pass
		GND	Pass	Pass
-14		+VOUT	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]
+16.5		+VOUT	Pass	Pass
		GND	Pass	Pass
-16.5		+VOUT	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]

[1]Power supply might initiate Auto-Restart or Hard Reset due to either:

- USB PD Controller protection, or
- USB-C power adapter tester Tiny-PAT protection at the load

18.2 *Air Discharge, CC1 and CC2, 230 VAC Input*

Discharge Voltage (kV)	ESD Strike Location		Test Result 20 V / 1.5 A
+8	End of Cable	CC1	Pass[1]
		CC2	Pass[1]
-8		CC1	Pass[1]
		CC2	Pass[1]
+10		CC1	Pass[1]
		CC2	Pass[1]
-10		CC1	Pass[1]
		CC2	Pass[1]
+12		CC1	Pass[1]
		CC2	Pass[1]
-12		CC1	Pass[1]
		CC2	Pass[1]
+14		CC1	Pass[1]
		CC2	Pass[1]
-14		CC1	Pass[1]
		CC2	Pass[1]
+16.5		CC1	Pass[1]
		CC2	Pass[1]
-16.5		CC1	Pass[1]
		CC2	Pass[1]
+8	On the Board	CC1	Pass[1]
		CC2	Pass[1]
-8		CC1	Pass[1]
		CC2	Pass[1]
+10		CC1	Pass[1]
		CC2	Pass[1]
-10		CC1	Pass[1]
		CC2	Pass[1]
+12		CC1	Pass[1]
		CC2	Pass[1]
-12		CC1	Pass[1]
		CC2	Pass[1]
+14		CC1	Pass[1]
		CC2	Pass[1]
-14		CC1	Pass[1]
		CC2	Pass[1]
+16.5		CC1	Pass[1]
		CC2	Pass[1]
-16.5		CC1	Pass[1]
		CC2	Pass[1]

[1]Power supply might initiate Auto-Restart or Hard Reset due to either:
- USB PD Controller protection, or
- USB-C power adapter tester Tiny-PAT protection at the load

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18.3 *Contact Discharge, +VOUT and GND, 230 VAC Input*

Discharge Voltage (kV)	ESD Strike Location		Test Result 5 V / 0 A	Test Result 20 V / 1.5 A
+8.0	End of Cable	+VOUT	Pass	Pass
		GND	Pass	Pass
-8.0		+VOUT	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]
+8.8		+VOUT	Pass	Pass
		GND	Pass	Pass
-8.8		+VOUT	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]
+8.0	On the Board	+VOUT	Pass	Pass
		GND	Pass	Pass
-8.0		+VOUT	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]
+8.8		+VOUT	Pass	Pass
		GND	Pass	Pass
-8.8		+VOUT	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]

[1]Power supply might initiate Auto-Restart or Hard Reset due to either:

- USB PD Controller protection, or
- USB-C power adapter tester Tiny-PAT protection at the load

18.4 *Contact Discharge, CC1 and CC2, 230 VAC Input*

Discharge Voltage (kV)	ESD Strike Location		Test Result 20 V / 1.5 A
+8.0	End of Cable	CC1	Pass[1]
		CC2	Pass[1]
-8.0		CC1	Pass[1]
		CC2	Pass[1]
+8.8		CC1	Pass[1]
		CC2	Pass[1]
-8.8		CC1	Pass[1]
		CC2	Pass[1]

[1]Power supply might initiate Auto-Restart or Hard Reset due to either:

- USB PD Controller protection, or
- USB-C power adapter tester Tiny-PAT protection at the load

19 Revision History

Date	Author	Revision	Description & Changes	Reviewed
24-Jul-20	DB	1.0	Initial Release.	Apps & Mktg
10-Aug-20	KM	1.1	Updated BOM with Alternates	Apps & Mktg
14-Aug-20	DB	1.2	Updated BOM	Apps & Mktg
19-Sep-20	DB	1.3	Updated Transformer construction, Thermal Performance, EMI, ESD, and board images.	Apps & Mktg

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