Design Example Report

Title	*15 W Low THD High Efficiency Non-Isolated Buck-boost, Universal Input LED Driver Using LYTSwitch™-4 LYT4213E*
Specification	95 VAC – 265 VAC Input; 200 V_{TYP}, 75 mA Output
Application	LED Tube Driver
Author	Applications Engineering Department
Document Number	DER-425
Date	March 11, 2015
Revision	1.0

Summary and Features

- Single-stage power factor correction combined with constant current (CC) output
- Universal Input Voltage
- Integrated protection and reliability features
  - Output short-circuit protected with auto-recovery
  - Auto-recovering thermal shutdown with large hysteresis
  - No damage during brown-out conditions
- PF >0.9 at 115 VAC and 230 VAC
- THD <15% at 115 VAC and 230 VAC
- Meets ring wave and differential line surge and EN55015 conducted EMI

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Important Note: Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This document describes a non-isolated, high power factor (PF), low THD LED driver designed to drive a nominal LED string voltage of 200 V at 75 mA from an input voltage range of 95 VAC to 265 VAC (50 Hz typical). The LED driver utilizes the LYT4213E from the LYTSwitch-4 family of ICs.

The topology used is a single-stage non-isolated buck-boost that meets high power factor, constant current regulation, and low THD requirements for the application.

This document contains the LED driver specification, schematic, PCB details, bill of materials, transformer documentation and typical performance characteristics.

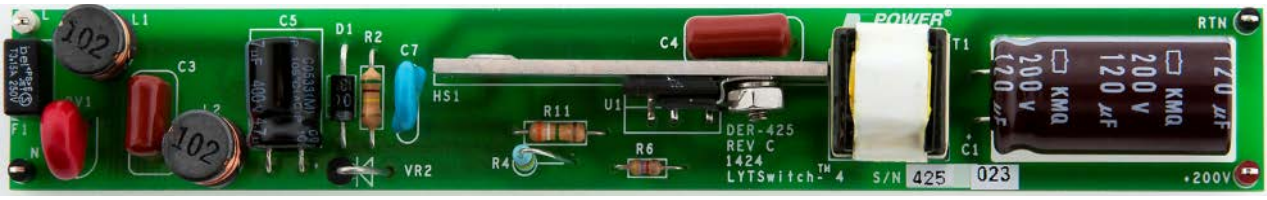

Figure 1 – Populated Circuit Board, Top View.

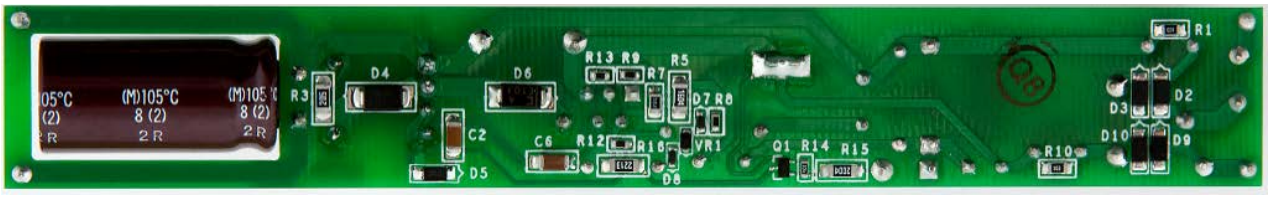

Figure 2 – Populated Circuit Board, Bottom View.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	95	115/230	265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}		50/60		Hz	
Output						
Output Voltage	V_{OUT}		200		V	
Output Current	I_{OUT}		75		mA	
Total Output Power						
Continuous Output Power	P_{OUT}		15		W	
Efficiency						
Full Load, 115 VAC	η		>86		%	Measured at P_{OUT} 25 °C
Full Load, 230 VAC	η		>89		%	Measured at P_{OUT} 25 °C
Environmental						
Conducted EMI			CISPR 15B / EN55015B			
Safety			Non-Isolated			
Ring Wave (100 kHz)			2.5		kV	
Differential Mode (L1-L2)			1.0		kV	
Power Factor			0.9			Measured at $V_{OUT(TYP)}$, $I_{OUT(TYP)}$ and 120 VAC, 50 Hz
Ambient Temperature	T_{AMB}		30		°C	Free convection, sea level

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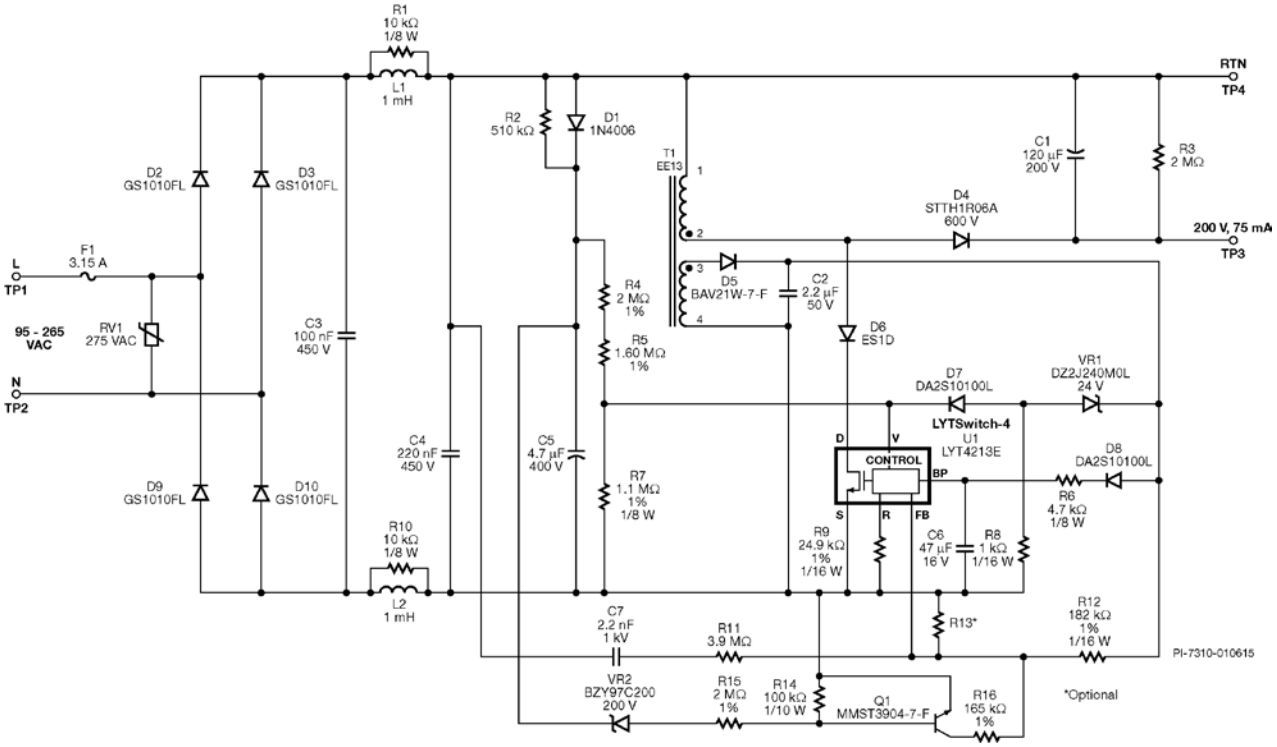
3 Schematic



*optional component

Figure 3 – Schematic.

4 Circuit Description

The LYTSwitch-4 family of devices are single-stage, power factor corrected controllers with a monolithically integrated 725 V power MOSFET, for use in LED driver applications. The LYT4213E IC is a member of the LYTSwitch-4 low line family and for this design, was configured as a single-stage buck-boost LED driver. The design provides a regulated constant current output while maintaining high power factor and low THD from a universal AC mains input.

4.1 Input EMI Filtering

Diode D2, D3, D9 and D10 rectify the AC input to provide a pulsating DC across the π filter consisting of C3, C4, L1 and L2. Resistor R1 and R2 are connected across L1 and L2 to damp any LC resonance which may cause EMI. Fuse F1 provides protection from any component failure and RV1 clamps the maximum voltage at the input during differential surge events.

4.2 Power Circuit

A low-side buck-boost topology was used to provide a THD less than 15% across the universal input range.

Output diode D4 conducts and rectifies the voltage from pin 2 of T1 every time the MOSFET of U1 turns off and the energy stored in inductor T1 is transferred to the load. Capacitor C1 is a filter that smooths the voltage and current delivered to the load. Diode D6 is a blocking diode that prevents reverse current from flowing through U1 when the voltage across C4 falls below the output voltage close to the zero crossing of the input AC voltage.

Peak line voltage information needed by U1 for regulation as well as power factor correction is provided via the peak detect circuit consisting of R2, D1, and C5. Current will flow to the VOLTAGE MONITOR (V) pin from C5 voltage through R4 and R5. R7 was used to fine tune the output current regulation across the input voltage range (line regulation).

Line overvoltage shutdown protection is also provided via the V pin of U1. Once the overvoltage current threshold (IOV) is exceeded (due to surge or line swell) U1 switching is inhibited, thus limiting the voltage stress to below the BV_{DSS} rating of the internal power MOSFET.

Capacitor C6 provides local decoupling for the BP pin of U1 which is the supply pin for the internal controller. During start-up, C6 is charged to ~6 V from an internal high-voltage current source connected to the Drain of U1. Capacitor C6 is also chosen to be 47 μF to enable the device to operate on Reduced Power mode.

The REFERENCE pin of U1 is tied to ground (SOURCE) via 24.9 kΩ resistor R9.

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4.3 Output Feedback

The bias winding acts as a feedback winding which is filtered by the network consisting of D5 and C2. The voltage across the bias circuit results in a current flowing through R12 to the LYT4213E FEEDBACK pin. This information is used by the IC to set the output current of the LED driver. Resistor R13 serves as a fine tuning resistor to center the output current.

4.4 Bias Voltage and Open LED Protection

The voltage across C2 serves as an external bias supply connected in parallel to C6 through R6 and D8 to increase the LED driver's efficiency.

Zener diode VR1 and D7 provide open LED-string protection. Resistor R8 serves as a bleeder for any leakage current through VR1 during normal operation which prevents premature triggering. Voltage across the bias winding will increase due to an open LED string which increases current flow to the VOLTAGE MONITOR (V) pin of LYT4213E sending the device into skip-cycle operation once IOV threshold is exceeded.

4.5 R-C THD Feed-Forward

An RC network (R11 and C7 - see schematic) connected between input bus and FB pin of the IC provides current to the FB pin. The input to this pin is a modulated signal (I_{FB}) proportional to the rectified sinusoid input voltage. As I_{FB} changes with input voltage, the input current follows this change but still maintains average output power. This makes the input current more sinusoidal and reduces distortion. With the RC compensation network connected, the output current (computed by PIXIs) will change, even if the average I_{FB} is the same with and without this compensation circuit. This network should therefore be added before optimizing for regulation, manually iterating the values of R11 and C7 as necessary to get the desired average output current.

The value of C7 must be high enough to reduce the phase difference between the rectified input and I_{FB} input to obtain good THD performance. In this design example 2.2 nf was sufficient for high line input. The maximum DC voltage reached by C7 for buck-boost design occurs at maximum input voltage and maximum output voltage. It can be calculated as:

For buck-boost (also applicable to flyback):

$$V_{CF(BUCKBOOST(MAX))} = \frac{2}{\pi} \times \sqrt{2} \times V_{IN(RMS)(MAX)}$$

Resistor R11 value is limited by two IC parameters, $I_{FB(SKIP)}$ and $I_{FB(AR)}$. The R11 value should be equal or higher than the resistances $R_{F(AR)}$ and $R_{F(SKIP)}$.

To maintain the operating I_{FB} below $I_{FB(SKIP)}$, the peak current in R11 should be limited to $I_{RF(PK)}$.

$$I_{RF(PK)} = I_{FB(SKIP)} - I_{FB(MAX)}$$

Where: $I_{FB(MAX)}$ is the maximum operating I_{FB} which occurs at the maximum output voltage.

For a feedback using the bias winding:

$$I_{FB(MAX)} = \frac{(V_{OUT(MAX)} + V_D) \times \frac{N_B}{N_S} - V_{DB} - V_{FB}}{R_{FB}}$$

Where:
V_D is the output diode forward voltage drop.
V_{DB} is the bias winding forward voltage drop.
N_B and N_S is the number of turns for the bias and secondary winding respectively.

For more information regarding a technique for achieving low THD for LYTSwitch-4, please contact your local PI representative.

4.6 FB Current Offset Circuit

Zener diode VR2, resistors R15, R14, R16 and transistor Q1 form an offsetting current circuit on the feedback to shift the level of the output current into the FEEDBACK pin lower when operating at high input voltage. Once a certain input voltage is reached or when voltage across C4 exceeds the VR2 threshold, VR2 will drive Q1 on, and diverts current from the FEEDBACK pin through R16.

The offset current is set by:

$$I_{OFFSET} = \frac{2.3\ V}{R16}$$

The offset circuit makes the output current to stay within regulation at highline:

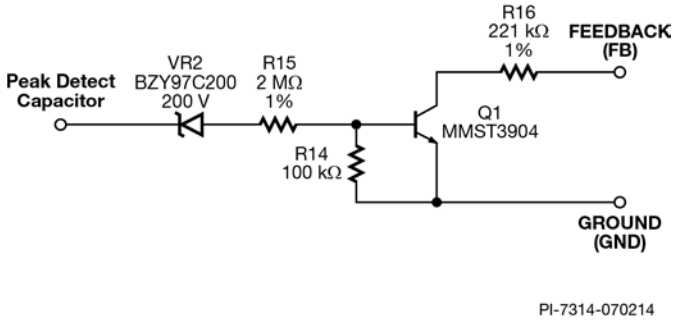

Figure 4 – FB Current Offset Circuit Schematic.

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5 PCB Layout

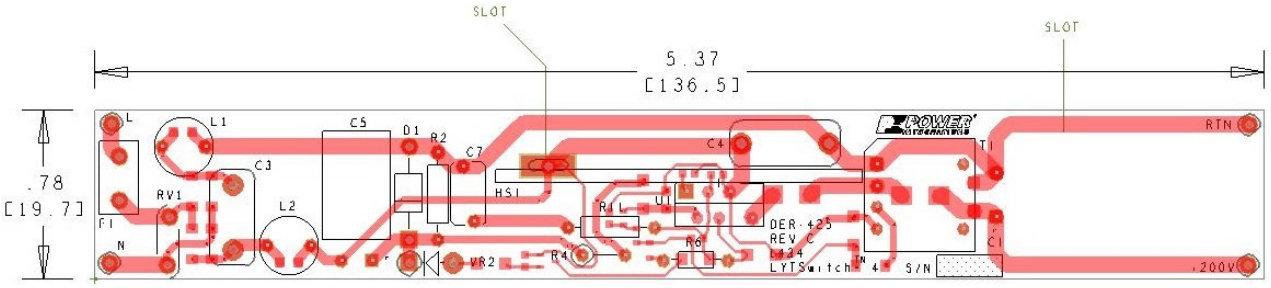

Figure 5 – Top Side.

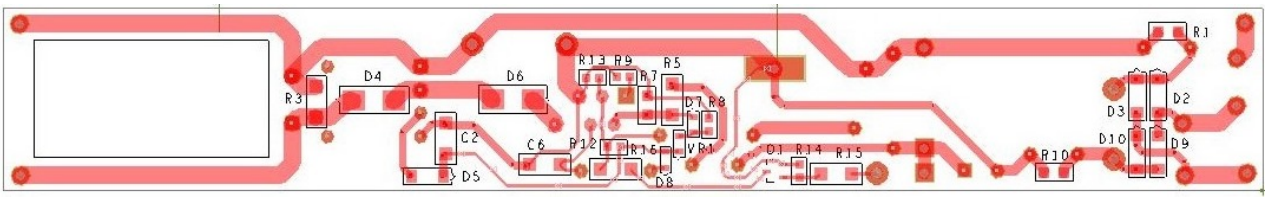

Figure 6 – Bottom Side.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	C1	120 μF, 200 V, Electrolytic, (12.5 x 25)	EKMQ201ELL121MK25S	Nippon Chemi-Con
2	1	C2	2.2 μF, 50 V, Ceramic, Y5V, 1206	UMK316F225ZG-T	Taiyo Yuden
3	1	C3	100 nF, 450 V, Film	MEXXD31004JJ1	Duratech
4	1	C4	220 nF, 450 V, Film	MEXXF32204JJ	Duratech
5	1	C5	4.7 μF, 400 V, Electrolytic, (8 x 11.5)	TAQ2G4R7MK0811MLL3	Taicon
6	1	C6	47 μF, 16 V, X5R, 1206	3216X5R1C476M	TDK
7	1	C7	2200 pF, 1 kV, Disc Ceramic	562R5GAD22	Vishay
8	1	D1	800 V, 1 A, GP, Rectifier, DO-41	1N4006-E3/54	Vishay
9	4	D2 D3 D9 D10	1000V, 1 A, Standard Recovery, SOD-123FL	GS1010FL	PanJit Semi
10	1	D4	600 V, 1 A, Ultrafast Recovery, 45 ns, DO-214AC, SMA	STTH1R06A	ST Micro
11	1	D5	250 V, 0.2 A, Fast Switching, 50 ns, SOD-123	BAV21W-7-F	Diodes, Inc.
12	1	D6	200 V, 1 A, Ultrafast Recovery, 25 ns, DO-214AC	ES1D-13-F	Diodes, Inc.
13	2	D7 D8	80 V, 0.1 A, Fast Switching, 3 ns, SSMini2	DA2S10100L	Panasonic
14	1	F1	3.15 A, 250 V, Slow, RST	507-1181	Belfuse
15	1	HS1	Heat Sink, Custom, Al, 3003, 0.062" Thk		Custom
16	2	L1 L2	1 mH, 0.30 A, Ferrite Core	CTCH895F-102K	CT Parts
17	1	Q1	NPN, Small Signal BJT, 40 V, 0.2 A, SOT-323	MMST3904-7-F	Diodes, Inc.
18	2	R1 R10	10 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ103V	Panasonic
19	1	R2	510 kΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-510K	Yageo
20	1	R3	2 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ205V	Panasonic
21	1	R4	2.00 MΩ, 1%, 1/4 W, Metal Film	RNF14FTD2M00	Stackpole
22	1	R5	1.60 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1604V	Panasonic
23	1	R6	4.7 kΩ, 5%, 1/8 W, Carbon Film	CF18JT4K70	Stackpole
24	1	R7	1.1 M, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1104V	Panasonic
25	1	R8	1 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1001V	Panasonic
26	1	R9	24.9 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2492V	Panasonic
27	1	R11	3.9 MΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-3M9	Yageo
28	1	R12	182 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1823V	Panasonic
29	1	R14	100 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ104V	Panasonic
30	1	R15	2.00 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
31	1	R16	165 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1653V	Panasonic
32	1	RV1	275 V, 23 J, 7 mm, RADIAL	V275LA4P	Littlefuse
33	1	T1	Bobbin, EE13, Horizontal, 8 pins Transformer	EE-13 (8PIN) SNX-R1746	Janohig Electronic Santronics
34	2	TP1 TP4	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone
35	1	TP2	Test Point, WHT, Miniature THRU-HOLE MOUNT	5002	Keystone
36	1	TP3	Test Point, RED, Miniature THRU-HOLE MOUNT	5000	Keystone
37	1	U1	LYTSwitch-4, eSIP-7C	LYT4213E	Power Integrations
38	1	VR1	Diode, Zener, 24 V, 200 MW, SMINI2	DZ2J240M0L	Panasonic
39	1	VR2	Diode, Zener, 200, V, 1.5 W, DO-41	BZY97C200-TR	Vishay

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7 Inductor Specification

7.1 Electrical Diagram

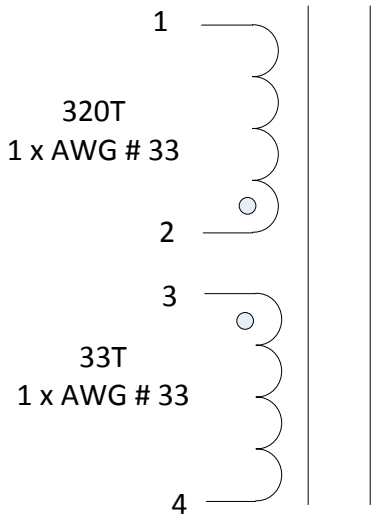

Figure 7 – Inductor Electrical Diagram.

7.2 Electrical Specifications

Primary Inductance	Pins 1-2, all other windings open, measured at 100 kHz, 0.4 RMS.	1.7 mH ±5%
Resonant Frequency	Pins 1-2, all other windings open.	800 kHz (Min.)

7.3 Materials

Item	Description
[1]	Core: TDK PC40EE13.
[2]	Bobbin: B-EE13-H-8pins-(4/4). PI p/n 25-01017-00; MFG p/n EE-13 (8 PIN).
[3]	Magnet Wire: #33 AWG.
[4]	Copper Tape: 50 um (2 mils) thick.
[5]	Tape: 3M 1298 Polyester Film, 7.7 mm wide.
[6]	Tape: 3M 1298 Polyester Film, 6.5 mm wide.

7.4 Inductor Build Diagram

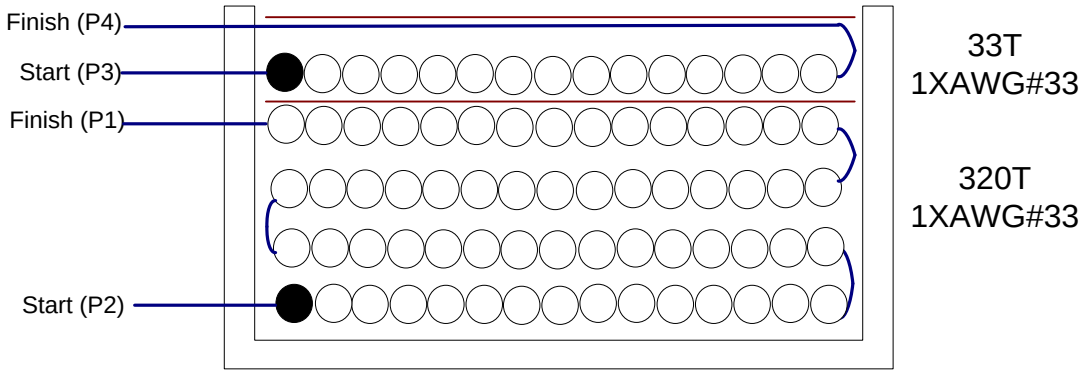

Figure 8 – Inductor Build Diagram.

7.5 Inductor Construction

Bobbin Preparation	Place the bobbin item [2] on the mandrel with pins 1-4 on the left.
Winding 1	Use wire item [3], start at pin 2 and wind 320 turns in clockwise direction. Terminate end of wire at pin 1.
Insulation	Fix with 1 layer tape item [5] for insulation.
Winding 2	Use wire item [3], start at pin 3 wind 33 turns in clockwise direction. Terminate wire at pin 4.
Insulation	Fix with 3 layers tape item [5] for insulation.
Finish	Grind core to achieve 1.7 mH inductance.
Assemble	Assemble and secure core halves with 3 layers of tape item [6]
Copper Shield	Add 1 turn of copper shield item [4] around core legs. Terminate shield to pin 4 using copper wire.
Pins	Cut pins 6 and 7.
Finish	Dip varnish transformer assembly.

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8 Inductor Design Spreadsheet

ACDC_LYTSwitch-4_080614; Rev.1.5; Copyright Power Integrations 2014	INPUT	INFO	OUTPUT	UNIT	LYTSwitch-4_080614: Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
Dimming required	NO		NO		Select 'YES' option if dimming is required. Otherwise select 'NO'.
VACMIN	90		90	V	Minimum AC Input Voltage
VACMAX	265	Warning	265	V	!!! Warning. VACMAX cannot be greater that 150 VAC
fL	50		50	Hz	AC Mains Frequency
VO	200.00		200.00	V	Typical output voltage of LED string at full load
VO_MAX	208.00		208.00	V	Maximum expected LED string Voltage.
VO_MIN	184.00		184.00	V	Minimum expected LED string Voltage.
V_OVP			228.80	V	Over-voltage protection setpoint
IO	0.075		0.075	A	Typical full load LED current
PO			15.0	W	Output Power
n	0.87		0.87		Estimated efficiency of operation
VB			20.00	V	Bias Voltage
ENTER LYTSwitch-4 VARIABLES					
LYTSwitch-4	LYT4X13		LYT4213		Selected LYTSwitch-4. Part number will change based on dimming/non-dimming application.
Current Limit Mode	RED		RED		Select "RED" for reduced Current Limit mode or "FULL" for Full current limit mode
ILIMITMIN			1	A	Minimum current limit
ILIMITMAX			1.16	A	Maximum current limit
fS			132000	Hz	Switching Frequency
fSmin			124000	Hz	Minimum Switching Frequency
fSmax			140000	Hz	Maximum Switching Frequency
IV			44.3	uA	V pin current
RV	3.60		3.60	M-ohms	Upper V pin resistor
RV2			1000000000000	M-ohms	Lower V pin resistor
IFB	131.80		131.80	uA	FB pin current (85 uA < IFB < 210 uA)
RFB1			129.0	k-ohms	FB pin resistor
VDS			10.00	V	LYTSwitch on-state Drain to Source Voltage
VD			0.50	V	Output Winding Diode Forward Voltage Drop (0.5 V for Schottky and 0.8 V for PN diode)
VDB			0.70	V	Bias Winding Diode Forward Voltage Drop
Key Design Parameters					
KP			0.80		Ripple to Peak Current Ratio (For PF > 0.9, 0.4 < KP < 0.9)
LP			1668	uH	Primary Inductance
VOR	200.00		200.00	V	Reflected Output Voltage.
Expected IO (average)			0.075	A	Expected Average Output Current
KP_VNOM			0.76		Expected ripple current ratio at VACNOM (115VAC)
TON_MIN			1.64	us	Minimum on time at maximum AC input voltage
PCLAMP			0.10	W	Estimated dissipation in primary clamp
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	EE13		EE13		Core Size
Custom Core					Enter custom core part number
AE			0.17	cm^2	Core Effective Cross Sectional Area
LE			3.02	cm	Core Effective Path Length
AL			1130	nH/T^2	Ungapped Core Effective Inductance
BW			7.4	mm	Bobbin Physical Winding Width
M			0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)

L	10		10		Number of Primary Layers
NS	320		320		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN			127	V	Peak input voltage at VACMIN
VMAX			375	V	Peak input voltage at VACMAX
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.63		Minimum duty cycle at peak of VACMIN
IAVG			0.15	A	Average Primary Current
IP			0.53	A	Peak Primary Current (calculated at minimum input voltage VACMIN)
IRMS			0.21	A	Primary RMS Current (calculated at minimum input voltage VACMIN)
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			1668	uH	Primary Inductance
LP_TOL			10		Tolerance of primary inductance
NP			319		Primary Winding Number of Turns
NB			33		Bias Winding Number of Turns
ALG			16	nH/T^2	Gapped Core Effective Inductance
BM			1622	Gauss	Maximum Flux Density at PO, VMIN (BM<3100)
BP			3545	Gauss	Peak Flux Density (BP<3700)
BAC			649	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1588		Relative Permeability of Ungapped Core
LG			1.29	mm	Gap Length (Lg > 0.1 mm)
BWE			74	mm	Effective Bobbin Width
OD			0.23	mm	Maximum Primary Wire Diameter including insulation
INS			0.05	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.19	mm	Bare conductor diameter
AWG			33	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			51	Cmils	Bare conductor effective area in circular mils
CMA			240	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 600)
TRANSFORMER SECONDARY DESIGN PARAMETERS (SINGLE OUTPUT EQUIVALENT)					
Lumped parameters					
ISP			0.53	A	Peak Secondary Current
ISRMS			0.15	A	Secondary RMS Current
IRIPPLE			0.13	A	Output Capacitor RMS Ripple Current
CMS			31	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			35	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			0.14	mm	Secondary Minimum Bare Conductor Diameter
ODS			0.02	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
VOLTAGE STRESS PARAMETERS					
VDRAIN		Warning	748	V	!!! REDUCE DRAIN VOLTAGE Vdrain<700, reduce VACMAX, reduce VOR
PIVS			605	V	Output Rectifier Maximum Peak Inverse Voltage (calculated at VOVP, excludes leakage inductance spike)
PIVB			62	V	Bias Rectifier Maximum Peak Inverse Voltage (calculated at VOVP, excludes leakage inductance spike)
FINE TUNING (Enter measured values from prototype)					
V pin Resistor Fine Tuning					
RV1			3.60	M-ohms	Upper V Pin Resistor Value
RV2			1000000000000	M-ohms	Lower V Pin Resistor Value
VAC1			115	V	Test Input Voltage Condition1
VAC2			230	V	Test Input Voltage Condition2

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IO_VAC1			0.075	A	Measured Output Current at VAC1
IO_VAC2			0.075	A	Measured Output Current at VAC2
RV1 (new)			3.60	M-ohms	New RV1
RV2 (new)			18820.47	M-ohms	New RV2
V_OV			287.9	V	Typical AC input voltage at which OV shutdown will be triggered
V_UV			60.0	V	Typical AC input voltage beyond which power supply can startup
FB pin resistor Fine Tuning					
RFB1			128.98	k-ohms	Upper FB Pin Resistor Value
RFB2			1000000000000	k-ohms	Lower FB Pin Resistor Value
VB1			18.35	V	Test Bias Voltage Condition1
VB2			20.83	V	Test Bias Voltage Condition2
IO1			0.075	A	Measured Output Current at Vb1
IO2			0.075	A	Measured Output Current at Vb2
RFB1 (new)			129.0	k-ohms	New RFB1
RFB2(new)			1000000000000	k-ohms	New RFB2
Input Current Harmonic Analysis					
Harmonic		Max Current	Limit		N/A
1st Harmonic		139.19	N/A	mA	N/A
3rd Harmonic		12.80	58.62	mA	PASS. 3rd Harmonic current content is lower than the limit
5th Harmonic		3.28	58.6	mA	PASS. 5th Harmonic current content is lower than the limit
7th Harmonic		1.28	58.6	mA	PASS. 7th Harmonic current content is lower than the limit
9th Harmonic		0.64	58.62	mA	PASS. 9th Harmonic current content is lower than the limit
11th Harmonic		0.38	58.62	mA	PASS. 11th Harmonic current content is lower than the limit
13th Harmonic		0.26	58.62	mA	PASS. 13th Harmonic current content is lower than the limit
15th Harmonic		0.20	58.62	mA	PASS. 15th Harmonic current content is lower than the limit
THD		9.5	%		Estimated total Harmonic Distortion (THD)

Notes:

- For a buck-boost topology, the PIXIs flyback spreadsheet can be used with the reflected voltage (VOR) set to the output voltage. The spreadsheet calculates the drain voltage and assumes a voltage-spike due to the leakage inductance present in a flyback topology. This leakage inductance is not present in a buck-boost topology since only one winding is involved.

- VDRAIN warning can be ignored, as actual worst case Drain voltage measured was 560 V peak (see above), which is within the internal MOSFET BV_{MAX} rating of 725 V.

9 Performance Data

All measurements were performed at room temperature using an LED load. The following data were measured using an LED load with 200 V output voltage. Refer to the table on Section 9.5 for complete test data.

9.1 Efficiency

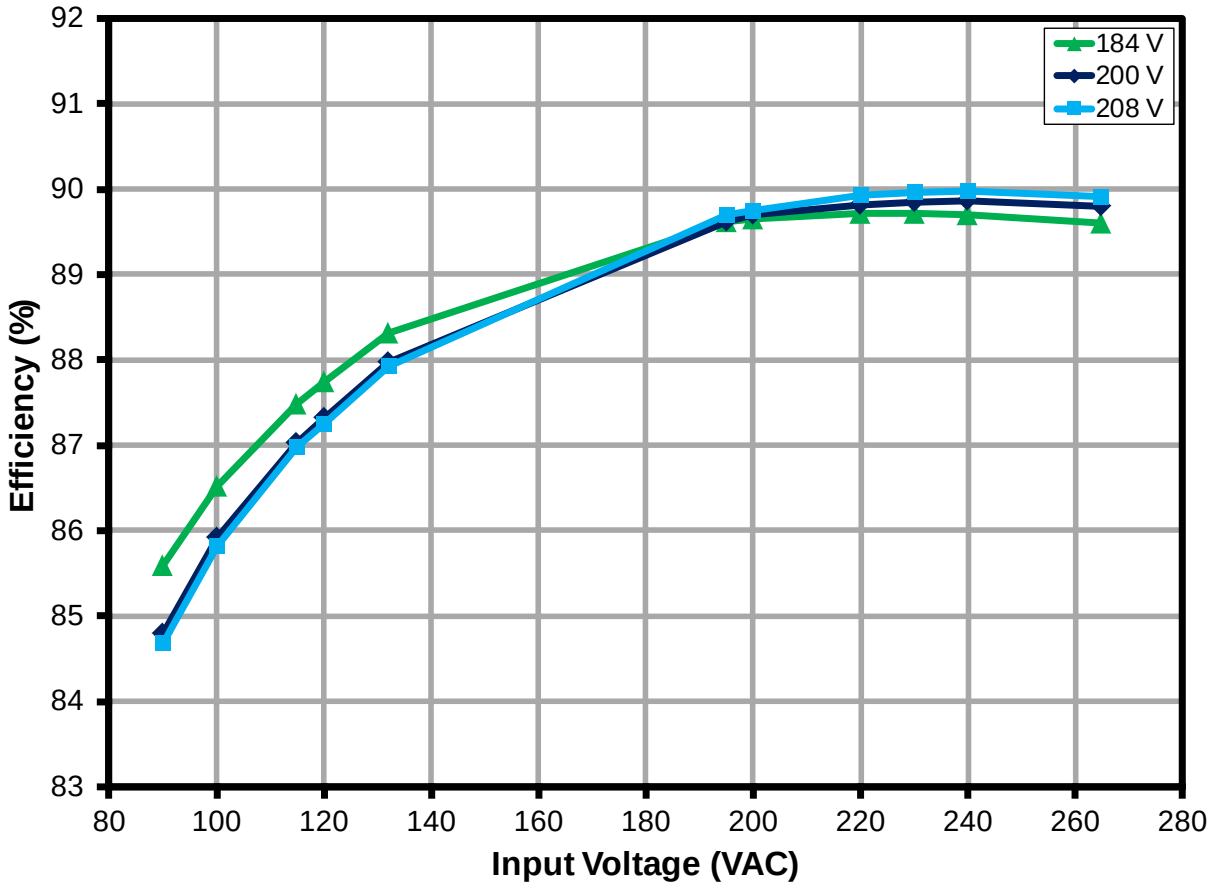

Figure 9 – Efficiency vs. Input Voltage.

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9.2 Line / Load Regulation

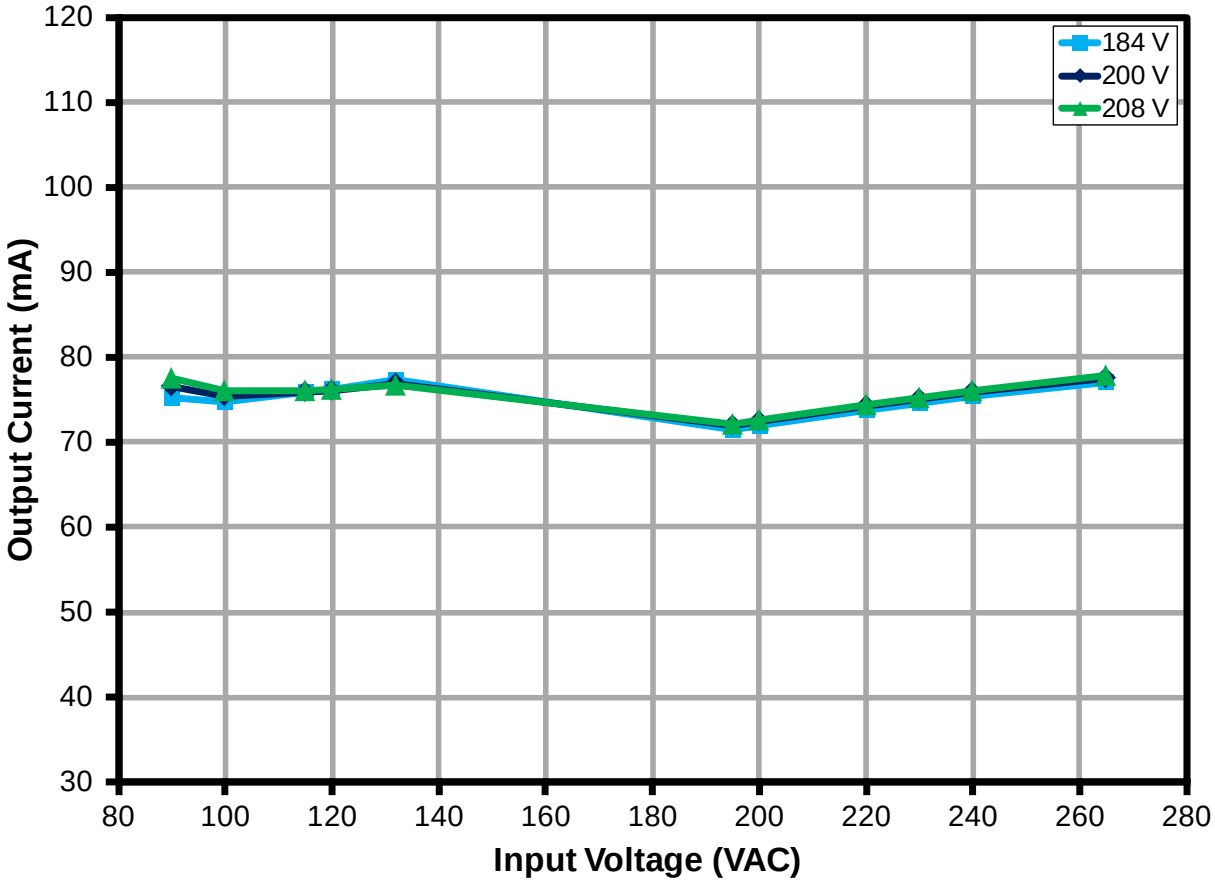

Figure 10 – Regulation vs. Line.

9.3 Power Factor

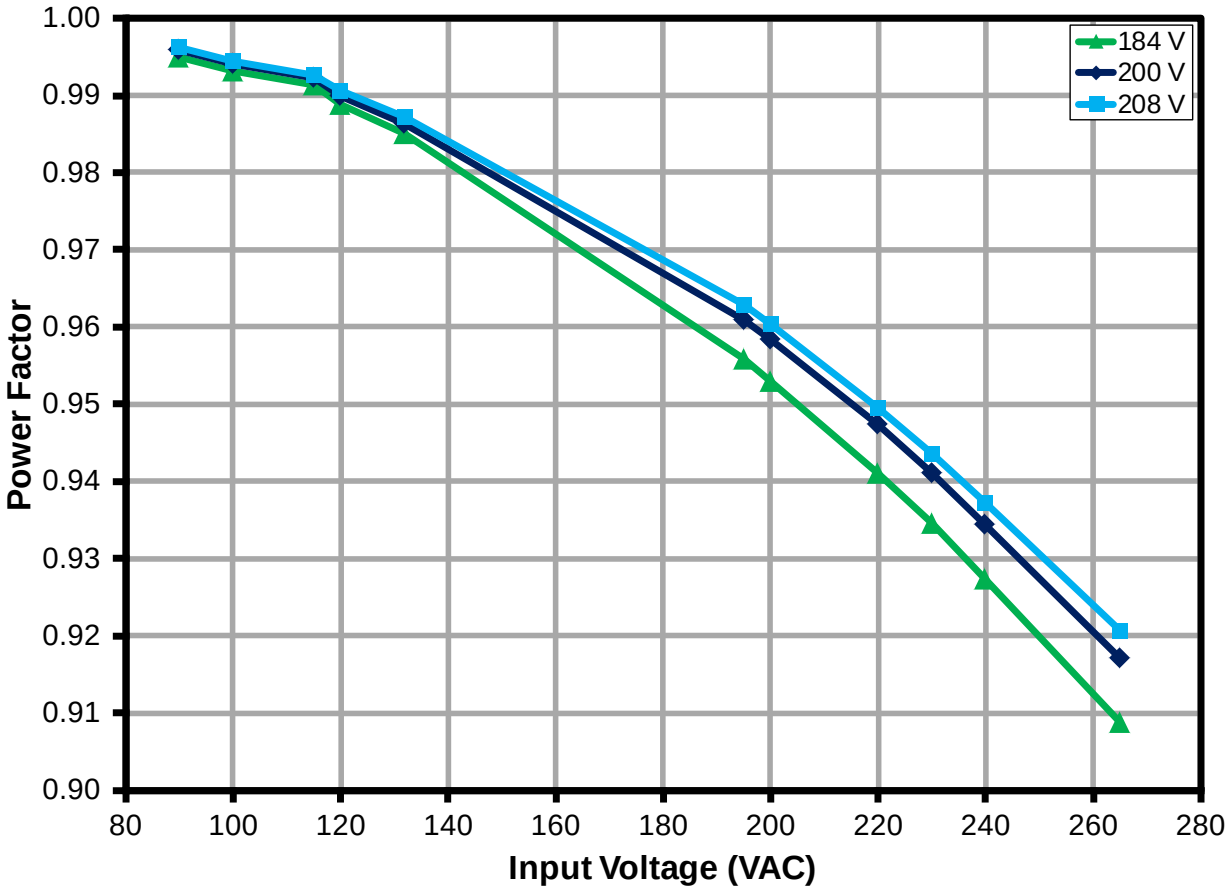

Figure 11 – Power Factor vs. Line.

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9.4 % ATHD

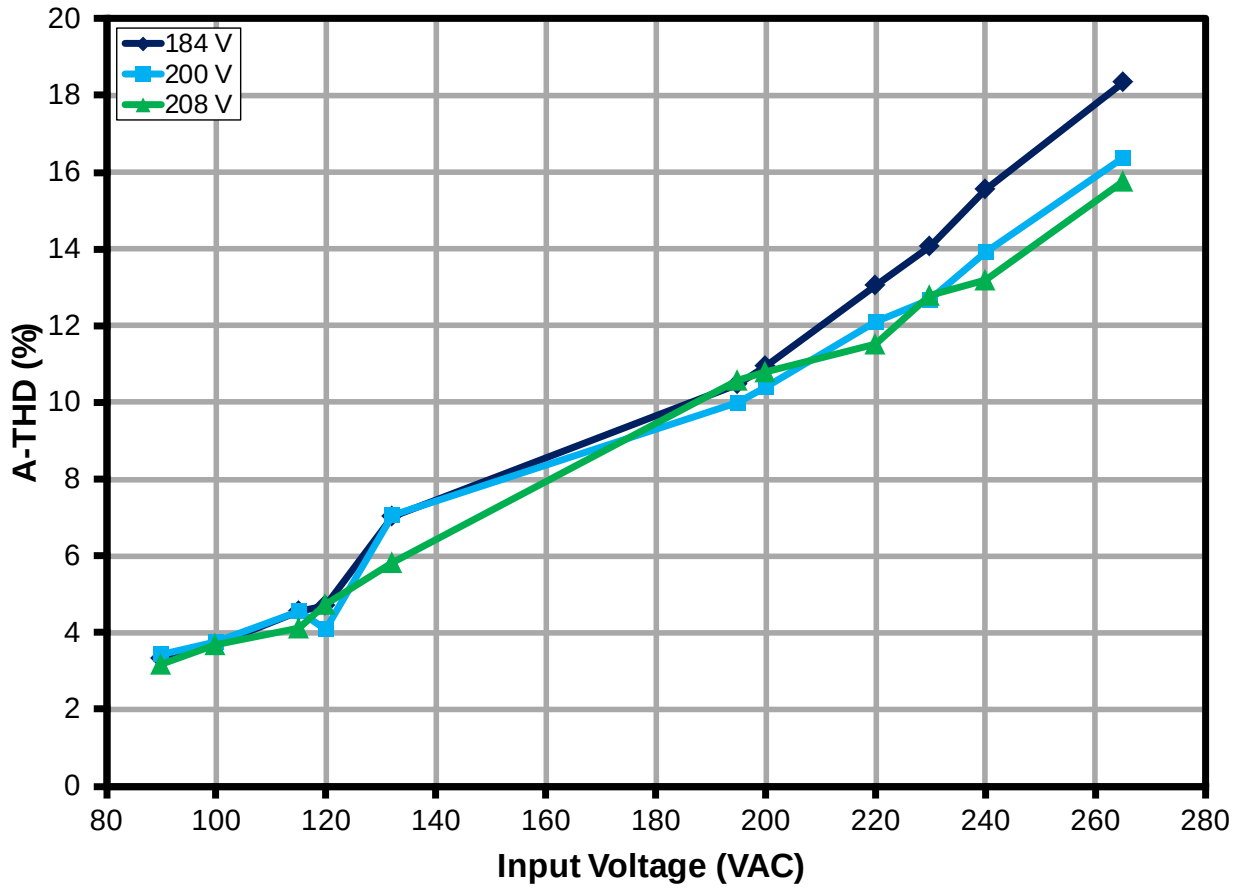

Figure 12 – % A-THD vs. Line for Different Output Voltages.

9.5 Input Current Harmonics

9.5.1 THD (Low-Line)

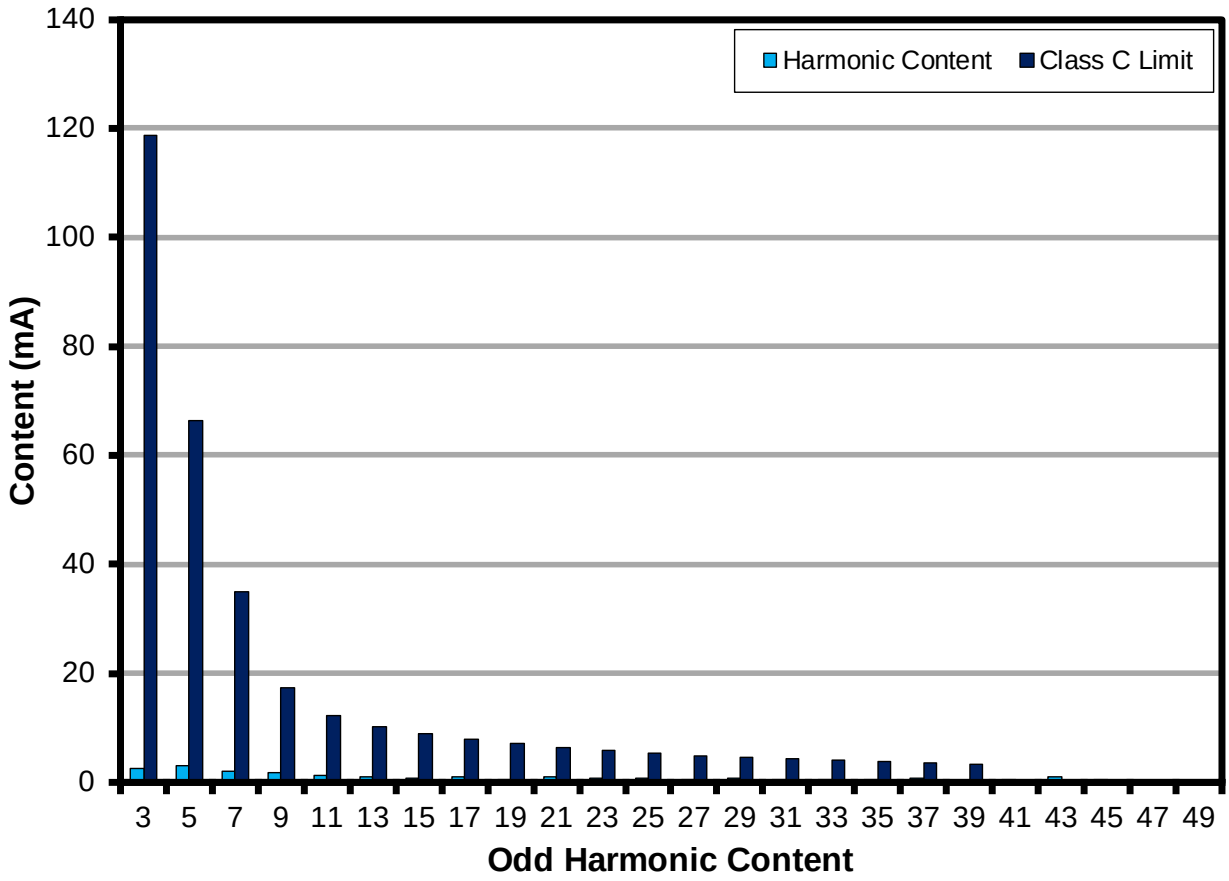

Figure 13 – Input Current Harmonics at 115 VAC for a 208 V LED Load.

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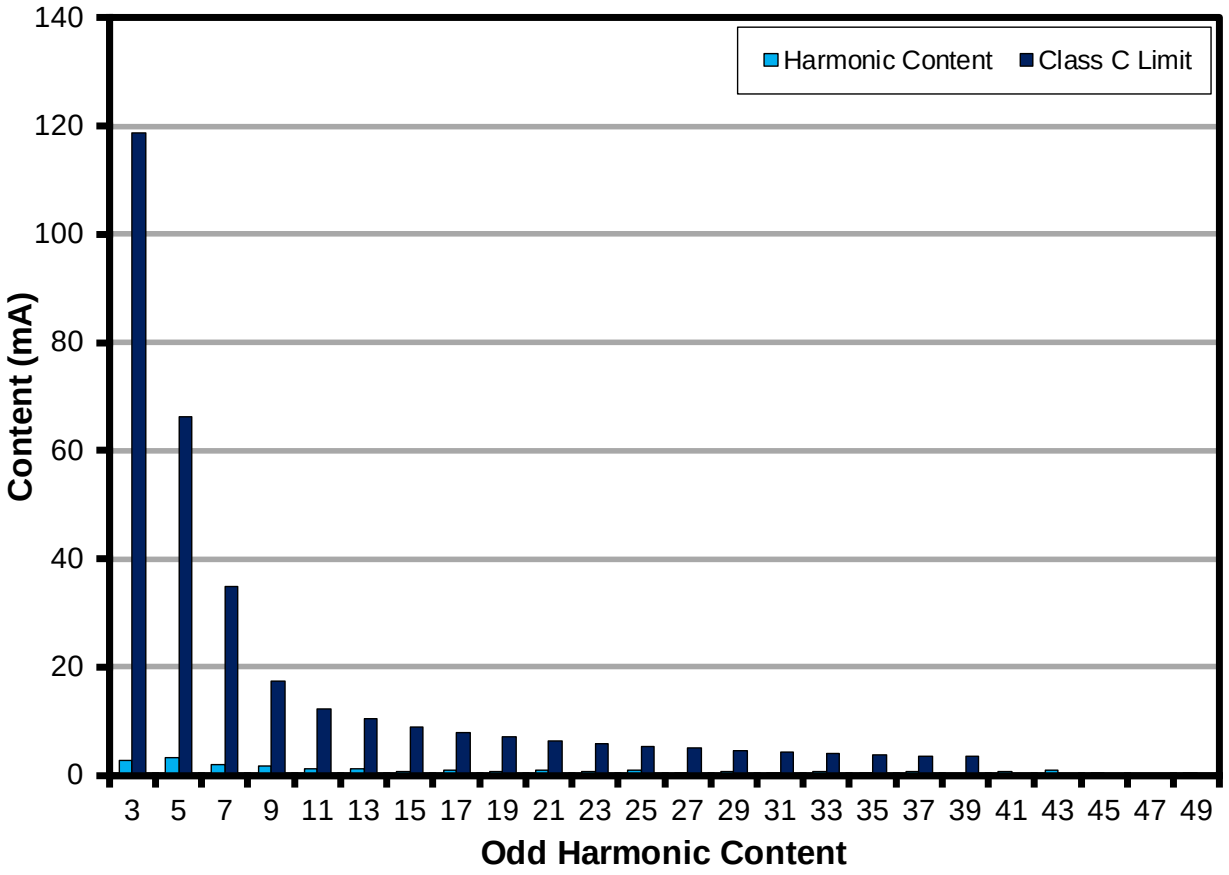

Figure 14 – Input Current Harmonics at 115 VAC for a 200 V LED Load.

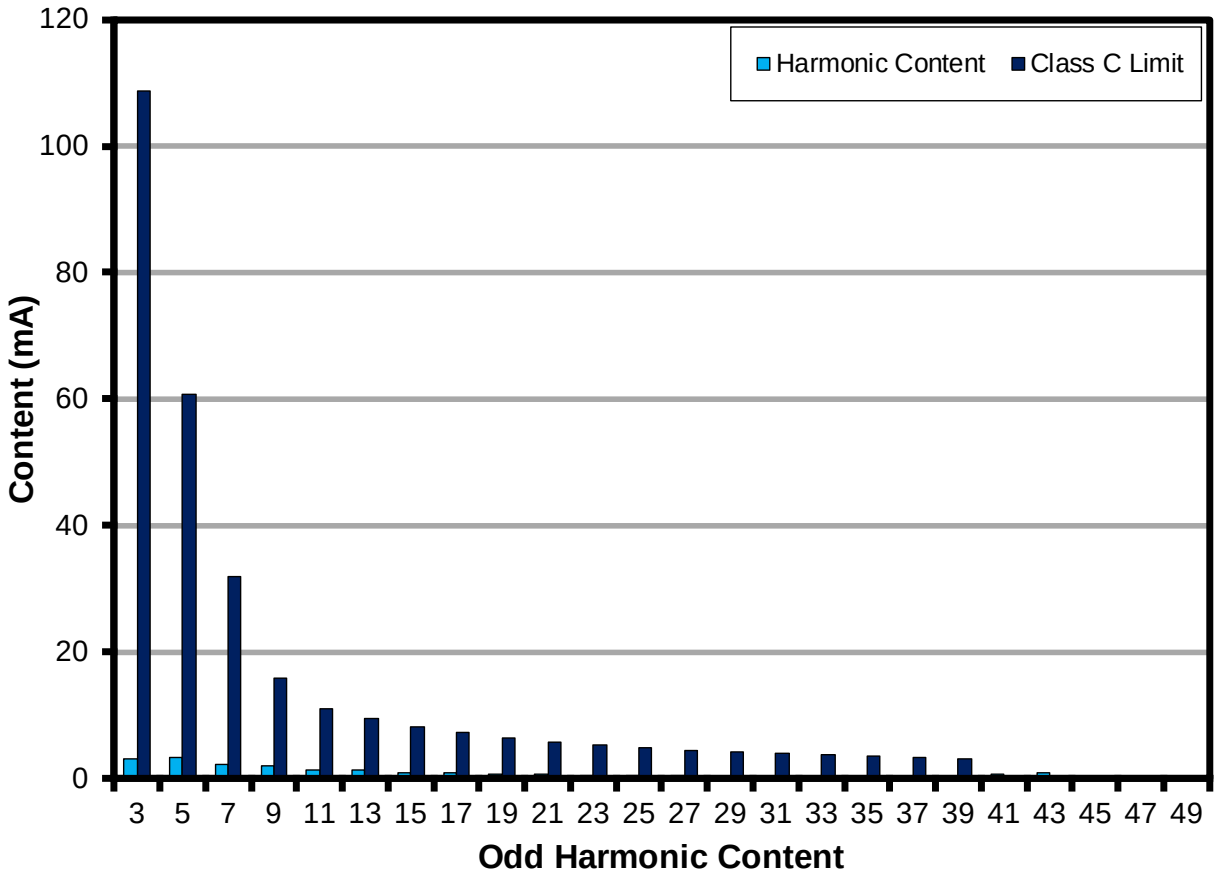

Figure 15 – Input Current Harmonics at 115 VAC for a 184 V LED Load.

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9.5.2 THD (High-Line)

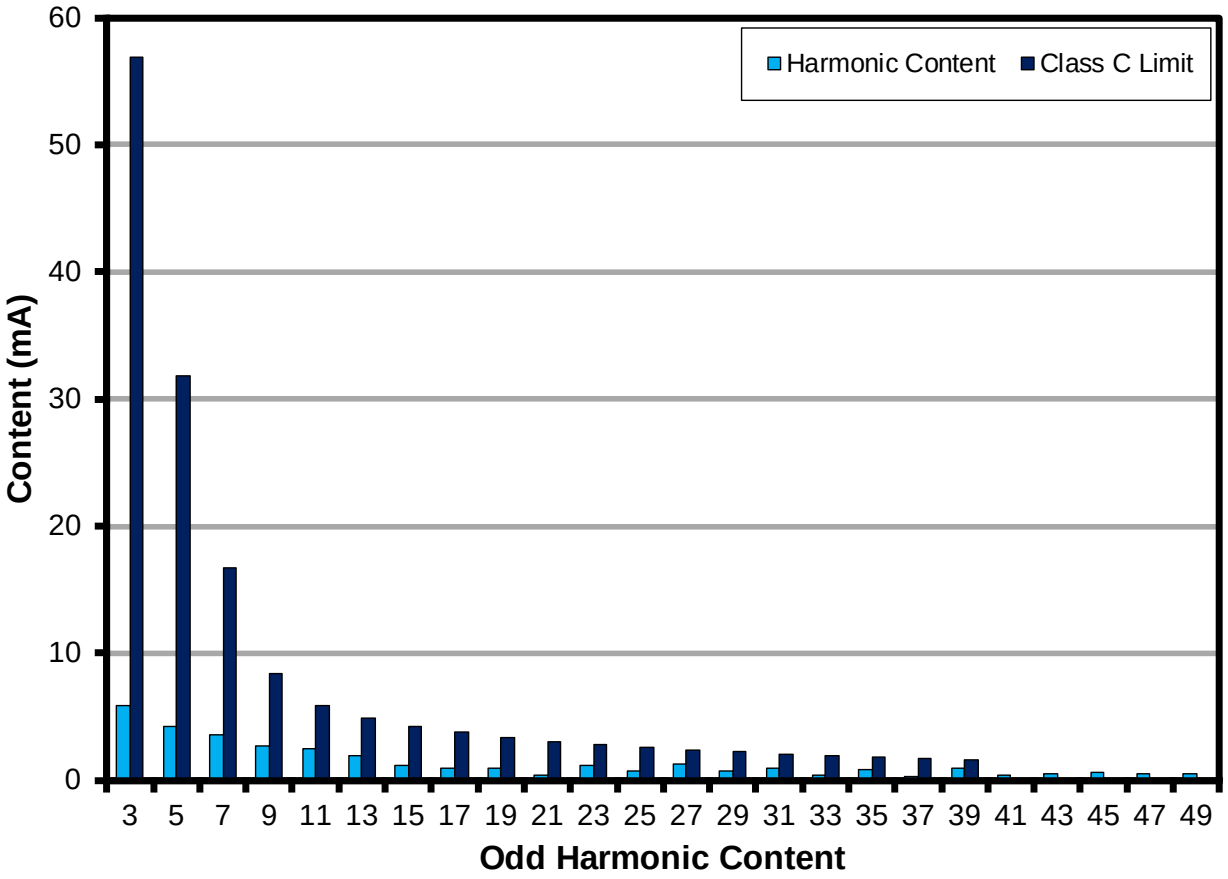

Figure 16 – Input Current Harmonics at 230 VAC for a 208 V LED Load

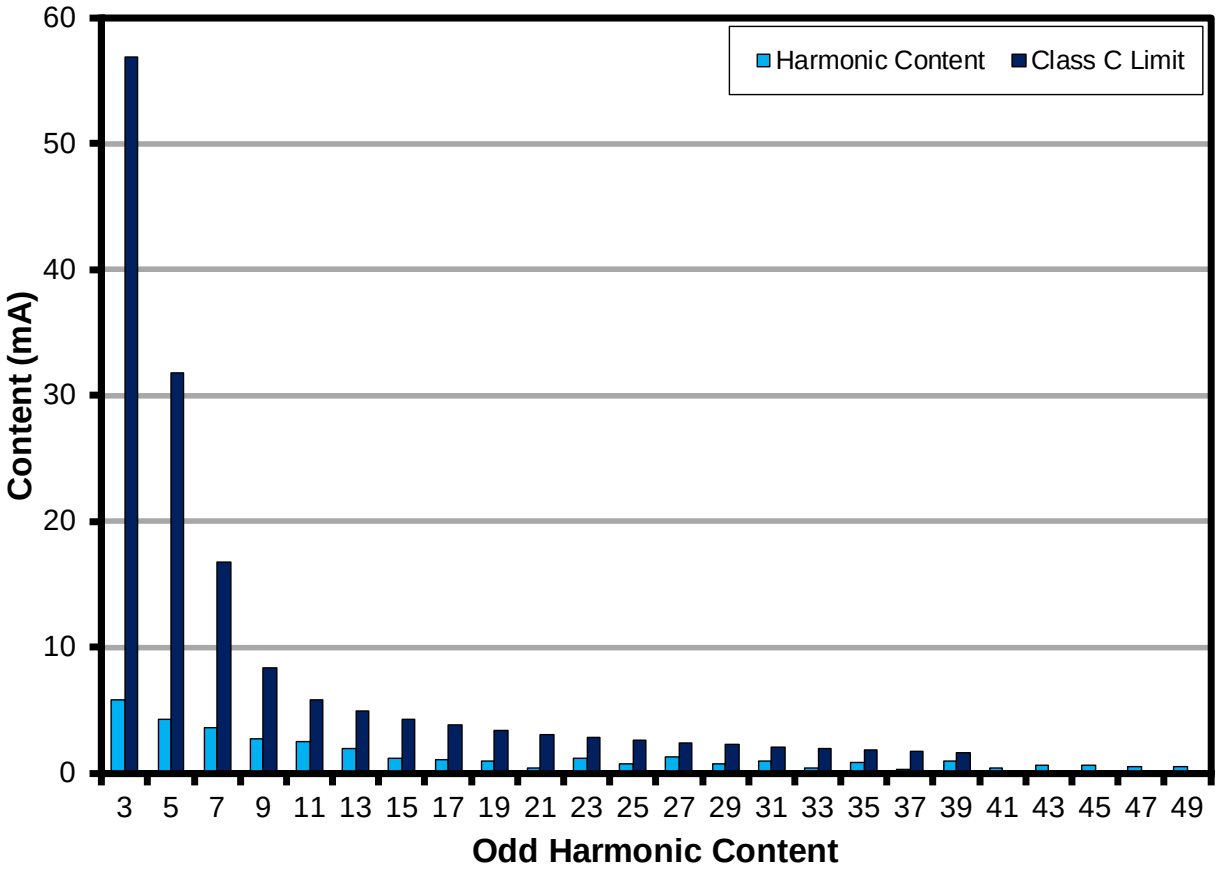

Figure 17 – Input Current Harmonics at 230 VAC for a 200 V LED Load.

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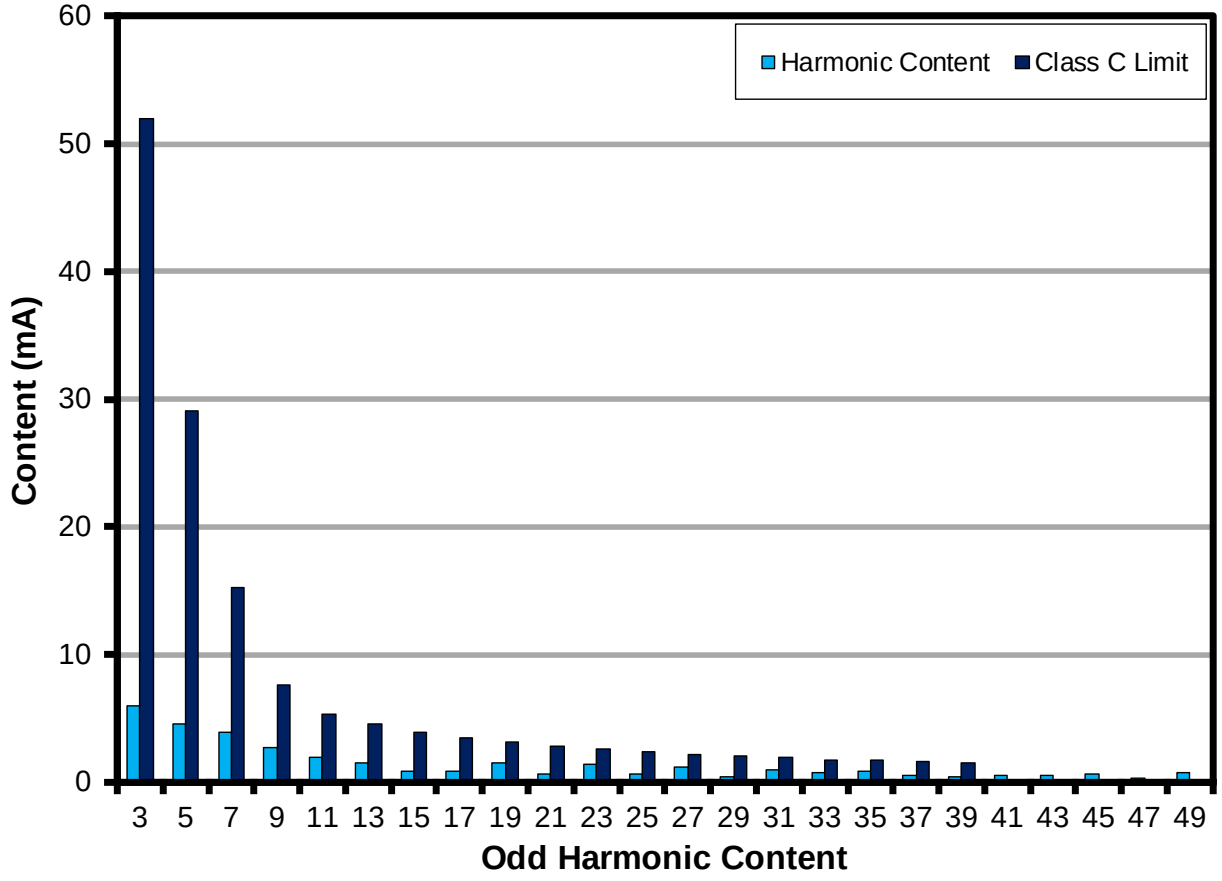

Figure 18 – Input Current Harmonics at 230 VAC for a 184 V LED Load.

9.6 Test Data

All measurements were taken with an open frame board, 25 ºC ambient, 50 Hz line frequency.

9.6.1 208 V LED Load

Input		Input Measurement					LED Load Measurement			Efficiency (%)
VAC (V_{RMS})	Freq (Hz)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	
90	60	90.0	213.4	19.13	1.00	3.2	208.8	77.6	16.2	84.7
100	60	100.0	185.5	18.45	0.99	3.7	208.3	76.0	15.8	85.8
115	60	115.0	159.7	18.23	0.99	4.1	208.4	76.1	15.9	87.0
120	60	119.9	153.1	18.19	0.99	4.7	208.4	76.2	15.9	87.3
132	60	132.0	139.6	18.19	0.99	5.8	208.5	76.7	16.0	87.9
195	50	195.0	88.8	16.67	0.96	10.6	207.3	72.2	15.0	89.7
200	50	200.0	87.3	16.77	0.96	10.8	207.4	72.6	15.1	89.8
220	50	220.0	82.4	17.22	0.95	11.5	207.9	74.5	15.5	89.9
230	50	230.0	80.3	17.41	0.94	12.8	208.1	75.3	15.7	90.0
240	50	240.0	78.3	17.61	0.94	13.2	208.3	76.1	15.9	90.0
265	50	265.0	74.1	18.07	0.92	15.8	208.8	77.8	16.3	89.9

9.6.2 200 V LED Load

Input		Input Measurement					LED Load Measurement			Efficiency (%)
VAC (V_{RMS})	Freq (Hz)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	
90	60	90.0	201.8	18.08	1.00	3.5	200.4	76.5	15.3	84.8
100	60	100.0	176.7	17.56	0.99	3.7	200.1	75.4	15.1	85.9
115	60	114.9	153.1	17.47	0.99	4.6	200.2	75.9	15.2	87.0
120	60	119.9	146.9	17.44	0.99	4.1	200.3	76.0	15.2	87.3
132	60	132.0	134.6	17.52	0.99	7.1	200.5	76.9	15.4	88.0
195	50	194.9	85.5	16.01	0.96	10.0	199.2	72.0	14.4	89.6
200	50	199.9	84.0	16.1	0.96	10.4	199.3	72.5	14.4	89.7
220	50	219.9	79.4	16.53	0.95	12.1	199.8	74.3	14.9	89.8
230	50	229.9	77.3	16.72	0.94	12.7	200.0	75.1	15.0	89.9
240	50	240.0	75.4	16.9	0.93	13.9	200.2	75.8	15.2	89.9
265	50	265.0	71.3	17.33	0.92	16.4	200.7	77.5	15.6	89.8

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9.6.3 184 V LED Load

Input		Input Measurement					LED Load Measurement			Efficiency (%)
VAC (V_{RMS})	Freq (Hz)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%ATHD	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	
90	60	89.9	180.6	16.16	1.00	3.3	184.0	75.2	13.8	85.6
100	60	100.0	160.0	15.88	0.99	3.7	183.9	74.7	13.7	86.5
115	60	114.9	140.2	15.98	0.99	4.6	184.2	75.9	14.0	87.5
120	60	119.9	135.0	16.01	0.99	4.7	184.2	76.2	14.1	87.7
132	60	132.0	124.3	16.16	0.99	7.0	184.5	77.3	14.3	88.3
195	50	194.9	78.4	14.6	0.96	10.5	183.1	71.5	13.1	89.6
200	50	199.9	77.2	14.7	0.95	10.9	183.2	71.9	13.2	89.7
220	50	219.9	73.0	15.11	0.94	13.1	183.6	73.8	13.6	89.7
230	50	229.9	71.2	15.3	0.93	14.1	183.9	74.6	13.7	89.7
240	50	239.9	69.5	15.47	0.93	15.5	184.0	75.4	13.9	89.7
265	50	264.9	65.9	15.86	0.91	18.3	184.4	77.0	14.2	89.6

9.6.4 208 V LED Load Harmonics Data

V	Freq	I (mA)	P	PF	%THD		V	Freq	I (mA)	P	PF	%THD
115.00	60.00	159.73	18.23	0.99	4.11		230.00	50.00	80.25	17.41	0.94	12.77
nth Order	**mA Content**	**% Content**	**Limit <25 W**	**Limit >25 W**	**Remarks**		**nth Order**	**mA Content**	**% Content**	**Limit <25 W**	**Limit >25 W**	**Remarks**
3	2.76	1.81%	123.96	29.78%	Pass		**3**	6.22	7.87%	59.21	28.31%	Pass
5	3.49	2.29%	69.27	10.00%	Pass		**5**	4.29	5.43%	33.09	10.00%	Pass
7	2.53	1.66%	36.46	7.00%	Pass		**7**	3.21	4.06%	17.41	7.00%	Pass
9	1.85	1.21%	18.23	5.00%	Pass		**9**	2.67	3.38%	8.71	5.00%	Pass
11	2.53	1.66%	12.76	3.00%	Pass		**11**	2.42	3.06%	6.09	3.00%	Pass
13	1.64	1.08%	10.80	3.00%	Pass		**13**	2.32	2.94%	5.16	3.00%	Pass
15	0.95	0.62%	9.36	3.00%	Pass		**15**	1.74	2.20%	4.47	3.00%	Pass
17	0.89	0.58%	8.26	3.00%	Pass		**17**	1.22	1.54%	3.94	3.00%	Pass
19	0.64	0.42%	7.39	3.00%	Pass		**19**	0.92	1.16%	3.53	3.00%	Pass
21	0.69	0.45%	6.68	3.00%	Pass		**21**	0.79	1.00%	3.19	3.00%	Pass
23	0.89	0.58%	6.10	3.00%	Pass		**23**	0.70	0.89%	2.91	3.00%	Pass
25	1.18	0.77%	5.61	3.00%	Pass		**25**	0.67	0.85%	2.68	3.00%	Pass
27	0.65	0.43%	5.20	3.00%	Pass		**27**	1.22	1.54%	2.48	3.00%	Pass
29	0.87	0.57%	4.84	3.00%	Pass		**29**	0.61	0.77%	2.31	3.00%	Pass
31	0.52	0.34%	4.53	3.00%	Pass		**31**	1.30	1.65%	2.16	3.00%	Pass
33	0.65	0.43%	4.25	3.00%	Pass		**33**	0.44	0.56%	2.03	3.00%	Pass
35	0.54	0.35%	4.01	3.00%	Pass		**35**	0.92	1.16%	1.92	3.00%	Pass
37	0.49	0.32%	3.79	3.00%	Pass		**37**	0.29	0.37%	1.81	3.00%	Pass
39	0.74	0.49%	3.60	3.00%	Pass		**39**	0.98	1.24%	1.72	3.00%	Pass
41	0.71	0.47%					**41**	0.36	0.46%			
43	0.75	0.49%					**43**	0.63	0.80%			
45	0.38	0.25%					**45**	0.55	0.70%			
47	0.54	0.35%					**47**	0.59	0.75%			
49	0.33	0.22%					**49**	0.74	0.94%			

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9.6.5 200 V LED Load Harmonics Data

V	Freq	I (mA)	P	PF	%THD		V	Freq	I (mA)	P	PF	%THD
115.00	60.00	153.14	17.47	0.99	4.56		230.00	50.00	77.28	16.72	0.94	12.67
nth Order	**mA Content**	**% Content**	**Limit <25 W**	**Limit >25 W**	**Remarks**		**nth Order**	**mA Content**	**% Content**	**Limit <25 W**	**Limit >25 W**	**Remarks**
3	2.66	1.82%	118.76	29.77%	Pass		**3**	5.86	7.71%	56.85	28.23%	Pass
5	3.20	2.19%	66.37	10.00%	Pass		**5**	4.23	5.56%	31.77	10.00%	Pass
7	1.96	1.34%	34.93	7.00%	Pass		**7**	3.57	4.70%	16.72	7.00%	Pass
9	1.79	1.22%	17.47	5.00%	Pass		**9**	2.76	3.63%	8.36	5.00%	Pass
11	1.18	0.81%	12.23	3.00%	Pass		**11**	2.48	3.26%	5.85	3.00%	Pass
13	1.14	0.78%	10.34	3.00%	Pass		**13**	1.94	2.55%	4.95	3.00%	Pass
15	0.73	0.50%	8.97	3.00%	Pass		**15**	1.14	1.50%	4.29	3.00%	Pass
17	1.03	0.70%	7.91	3.00%	Pass		**17**	1.01	1.33%	3.79	3.00%	Pass
19	0.60	0.41%	7.08	3.00%	Pass		**19**	0.91	1.20%	3.39	3.00%	Pass
21	0.91	0.62%	6.40	3.00%	Pass		**21**	0.45	0.59%	3.07	3.00%	Pass
23	0.66	0.45%	5.85	3.00%	Pass		**23**	1.18	1.55%	2.80	3.00%	Pass
25	0.82	0.56%	5.38	3.00%	Pass		**25**	0.78	1.03%	2.58	3.00%	Pass
27	0.50	0.34%	4.98	3.00%	Pass		**27**	1.26	1.66%	2.38	3.00%	Pass
29	0.75	0.51%	4.64	3.00%	Pass		**29**	0.70	0.92%	2.22	3.00%	Pass
31	0.44	0.30%	4.34	3.00%	Pass		**31**	0.99	1.30%	2.08	3.00%	Pass
33	0.57	0.39%	4.08	3.00%	Pass		**33**	0.44	0.58%	1.95	3.00%	Pass
35	0.48	0.33%	3.84	3.00%	Pass		**35**	0.84	1.10%	1.84	3.00%	Pass
37	0.67	0.46%	3.63	3.00%	Pass		**37**	0.30	0.39%	1.74	3.00%	Pass
39	0.29	0.20%	3.45	3.00%	Pass		**39**	0.92	1.21%	1.65	3.00%	Pass
41	0.62	0.42%					**41**	0.40	0.53%			
43	1.05	0.72%					**43**	0.57	0.75%			
45	0.55	0.38%					**45**	0.60	0.79%			
47	0.18	0.12%					**47**	0.52	0.68%			
49	0.33	0.23%					**49**	0.50	0.66%			

9.6.6 184 V LED Load Harmonics Data

V	Freq	I (mA)	P	PF	%THD		V	Freq	I (mA)	P	PF	%THD
115	60.00	140.23	15.98	0.99	4.57		230	50.00	71.21	15.30	0.93	14.07
nth Order	**mA Content**	**% Content**	**Limit <25 W**	**Limit >25 W**	**Remarks**		**nth Order**	**mA Content**	**% Content**	**Limit <25 W**	**Limit >25 W**	**Remarks**
3	3.31	2.48%	108.29	29.70%	Pass		**3**	6.03	8.63%	52.01	28.04%	Pass
5	3.60	2.70%	60.52	10.00%	Pass		**5**	4.54	6.50%	29.07	10.00%	Pass
7	2.76	2.07%	31.85	7.00%	Pass		**7**	3.92	5.61%	15.30	7.00%	Pass
9	2.08	1.56%	15.93	5.00%	Pass		**9**	2.69	3.85%	7.65	5.00%	Pass
11	2.89	2.17%	11.15	3.00%	Pass		**11**	1.95	2.79%	5.35	3.00%	Pass
13	1.16	0.87%	9.43	3.00%	Pass		**13**	1.55	2.22%	4.53	3.00%	Pass
15	1.33	1.00%	8.17	3.00%	Pass		**15**	0.90	1.29%	3.93	3.00%	Pass
17	0.61	0.46%	7.21	3.00%	Pass		**17**	0.81	1.16%	3.46	3.00%	Pass
19	0.31	0.23%	6.45	3.00%	Pass		**19**	1.47	2.10%	3.10	3.00%	Pass
21	0.27	0.20%	5.84	3.00%	Pass		**21**	0.68	0.97%	2.80	3.00%	Pass
23	0.93	0.70%	5.33	3.00%	Pass		**23**	1.43	2.05%	2.56	3.00%	Pass
25	0.64	0.48%	4.90	3.00%	Pass		**25**	0.70	1.00%	2.36	3.00%	Pass
27	0.57	0.43%	4.54	3.00%	Pass		**27**	1.20	1.72%	2.18	3.00%	Pass
29	0.17	0.13%	4.23	3.00%	Pass		**29**	0.42	0.60%	2.03	3.00%	Pass
31	0.24	0.18%	3.96	3.00%	Pass		**31**	0.95	1.36%	1.90	3.00%	Pass
33	0.30	0.22%	3.72	3.00%	Pass		**33**	0.72	1.03%	1.78	3.00%	Pass
35	0.26	0.19%	3.50	3.00%	Pass		**35**	0.86	1.23%	1.68	3.00%	Pass
37	0.45	0.34%	3.31	3.00%	Pass		**37**	0.50	0.72%	1.59	3.00%	Pass
39	0.37	0.28%	3.14	3.00%	Pass		**39**	0.46	0.66%	1.51	3.00%	Pass
41	0.55	0.41%					**41**	0.59	0.84%			
43	0.51	0.38%					**43**	0.53	0.76%			
45	0.55	0.41%					**45**	0.60	0.86%			
47	0.53	0.40%					**47**	0.34	0.49%			
49	0.54	0.40%					**49**	0.72	1.03%			

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10 Thermal Performance

Thermal measurements were taken in 25 ºC ambient temperature with a 200 V LED load.

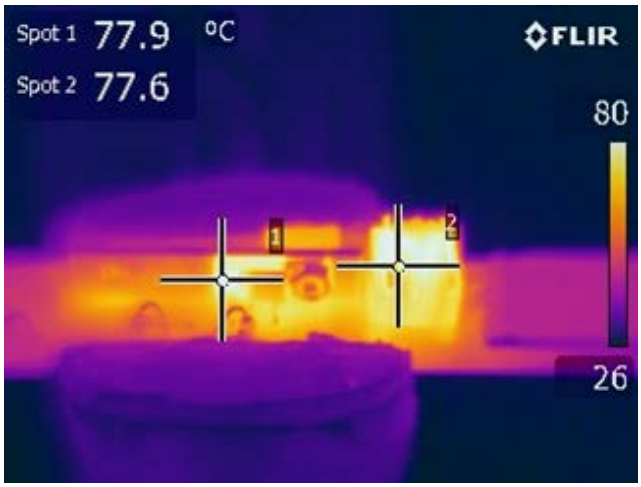

Figure 19 – 90 VAC, Full Load.
Spot 1: LYT4213E.
Spot 2: Tansformer.

Figure 20 – 115 VAC, Full Load.
Spot 1: LYT4213E.
Spot 2: Transformer.

Figure 21 – 230 VAC, Full Load.
Spot 1: LYT4213E.
Spot 2: Transformer.

Figure 22 – 265 VAC, Full Load.
Spot 1: LYT4213E.
Spot 2: Transformer.

11 Waveforms

11.1 Input Voltage and Input Current Waveforms

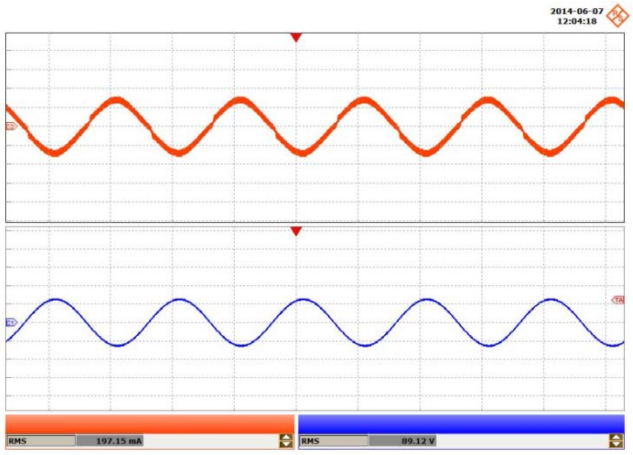

Figure 23 – 90 VAC, Full Load.
Upper: I_{IN}, 20 mA / div.
Lower: V_{IN}, 100 V, 10 ms / div.

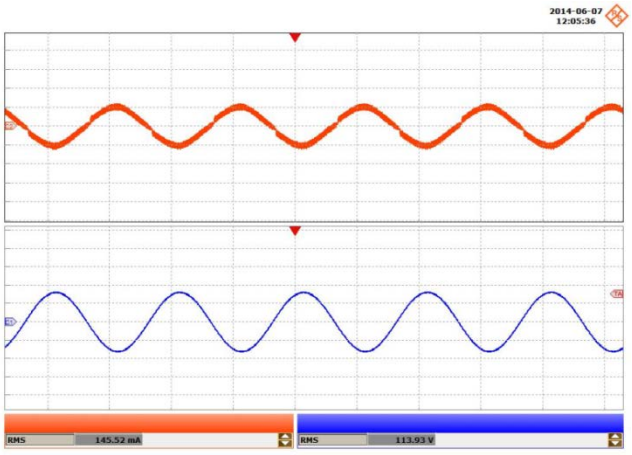

Figure 24 – 115 VAC, Full Load.
Upper: I_{IN}, 20 mA / div.
Lower: V_{IN}, 100 V, 10 ms / div.

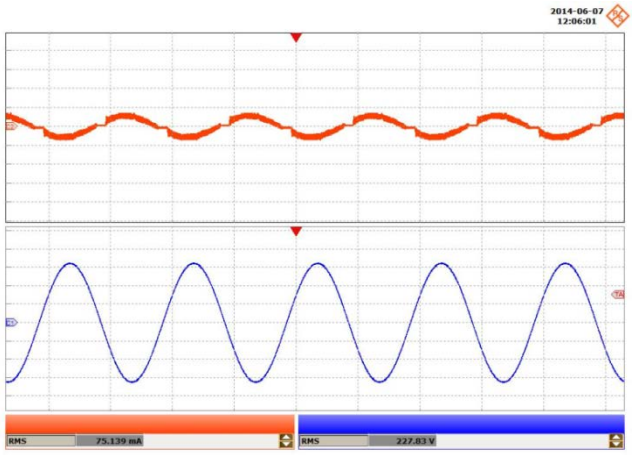

Figure 25 – 230 VAC, Full Load.
Upper: I_{IN}, 20 mA / div.
Lower: V_{IN}, 100 V, 10 ms / div.

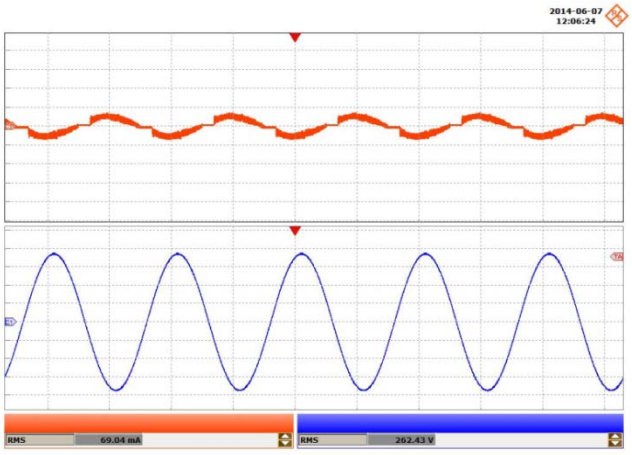

Figure 26 – 265 VAC, Full Load.
Upper: I_{IN}, 20 mA / div.
Lower: V_{IN}, 100 V, 10 ms / div.

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11.2 Output Current and Output Voltage at Normal Operation

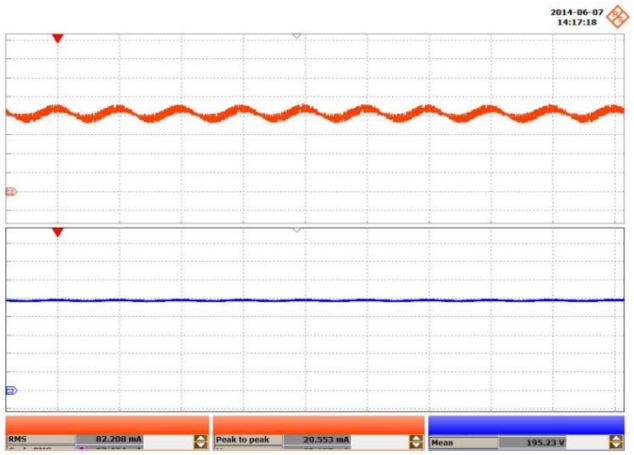

Figure 27 – 90 VAC, 50 Hz Full Load.
Upper: I_{OUT}, 20 mA / div.
Lower: V_{OUT}, 40 V, 10 ms / div.

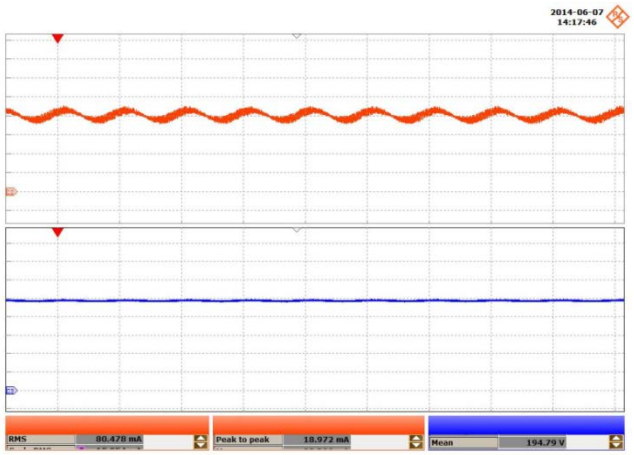

Figure 28 – 115 VAC, 50 Hz Full Load.
Upper: I_{OUT}, 20 mA / div.
Lower: V_{OUT}, 40 V, 10 ms / div.

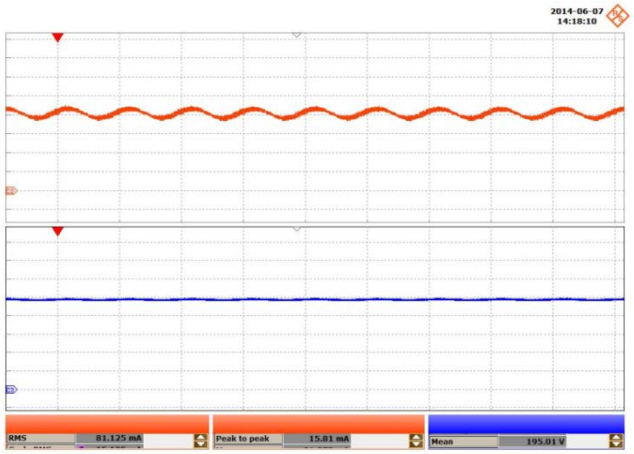

Figure 29 – 230 VAC, 50 Hz Full Load.
Upper: I_{OUT}, 20 mA / div.
Lower: V_{OUT}, 40 V, 10 ms / div.

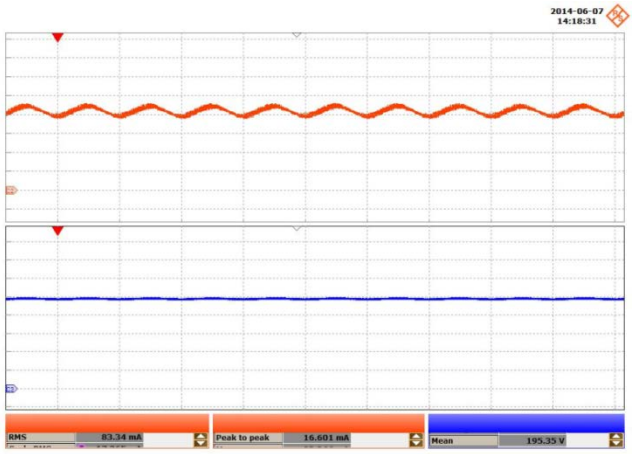

Figure 30 – 265 VAC, 50 Hz Full Load.
Upper: I_{OUT}, 20 mA / div.
Lower: V_{OUT}, 40 V, 10 ms / div.

11.3 Output Rise Time

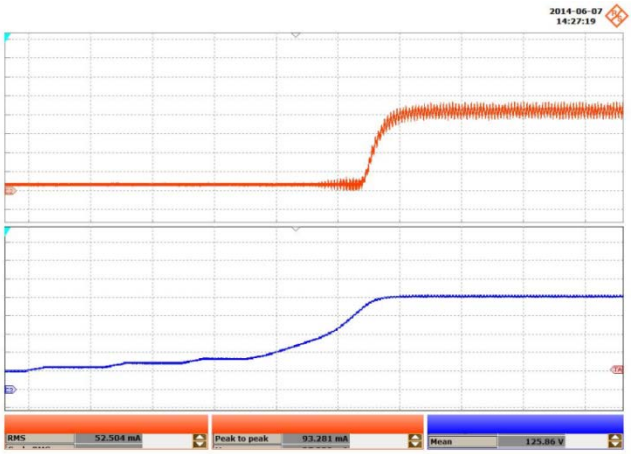

Figure 31 – 90 VAC Output Rise.
Upper: I_{OUT}, 20 mA / div.
Lower: V_{OUT} 40 V, 200 ms / div.

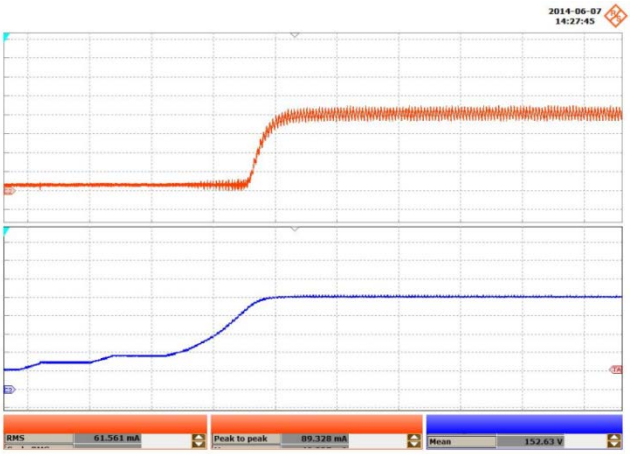

Figure 32 – 115 VAC Output Rise.
Upper: I_{OUT}, 20 mA / div.
Lower: V_{OUT}, 40 V, 200 ms / div.

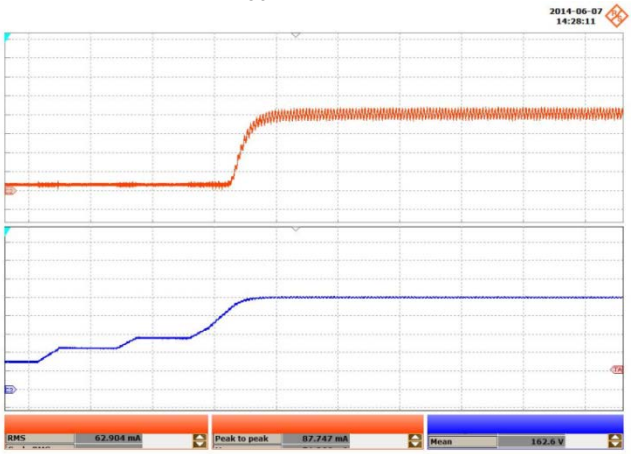

Figure 33 – 230 VAC Output Rise.
Upper: I_{OUT}, 20 mA / div.
Lower: V_{IN}, 40 V, 200 ms / div.

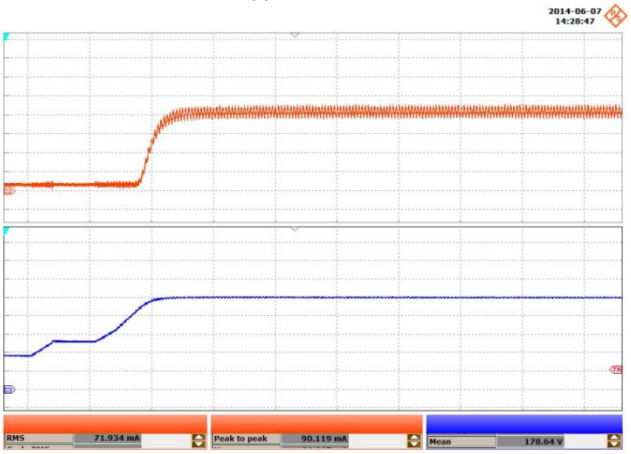

Figure 34 – 265 VAC Output Rise.
Upper: I_{OUT}, 20 mA / div.
Lower: V_{IN}, 40 V, 200 ms / div.

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11.4 Drain Voltage and Current at Normal Operation

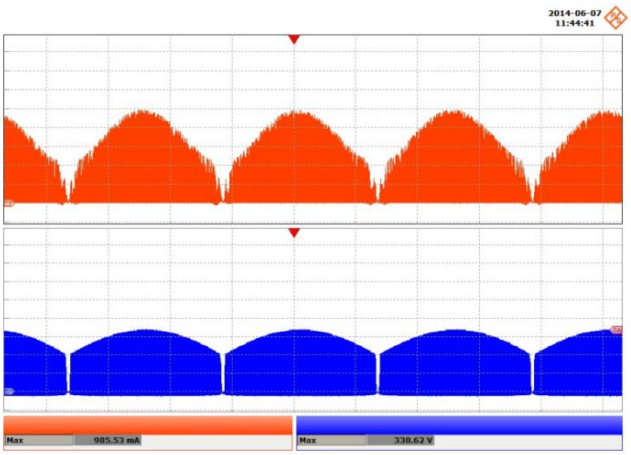

Figure 35 – 90 VAC, 50 Hz.
Upper: I_{DRAIN}, 0.2 A / div.
Lower: V_{DRAIN}, 100 V, 5 ms / div.

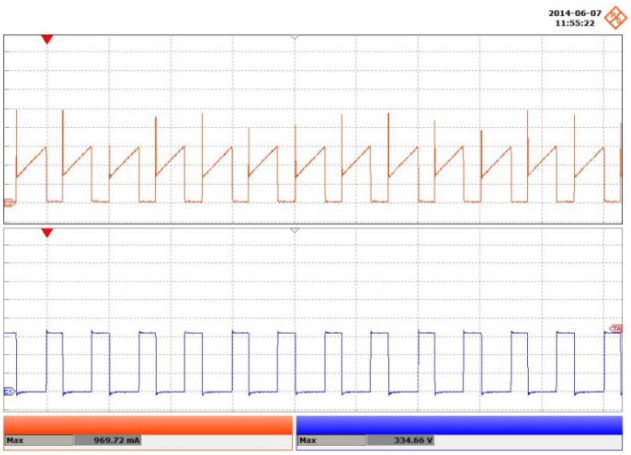

Figure 36 – 90 VAC, 50 Hz.
Upper: I_{DRAIN}, 0.2 A / div.
Lower: V_{DRAIN}, 100 V / div., 10 µs / div.

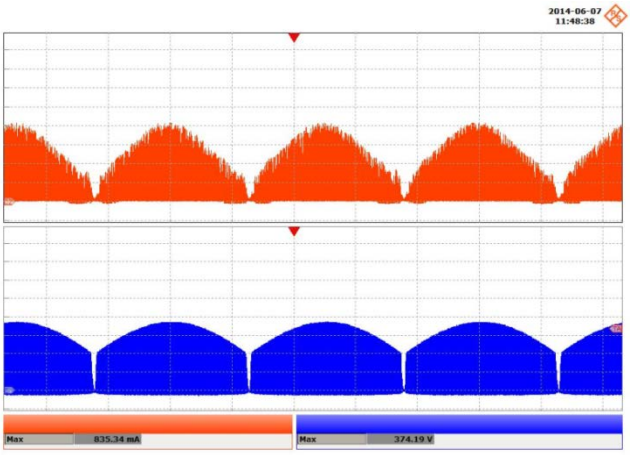

Figure 37 – 115 VAC, 50 Hz.
Upper: I_{DRAIN}, 0.2 A / div.
Lower: V_{DRAIN}, 100 V, 5 ms / div.

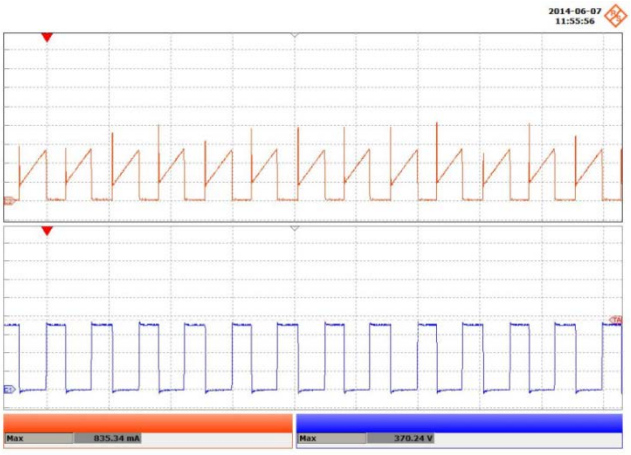

Figure 38 – 115 VAC, 50 Hz.
Upper: I_{DRAIN}, 0.2 A / div.
Lower: V_{DRAIN}, 100 V / div., 10 µs / div.

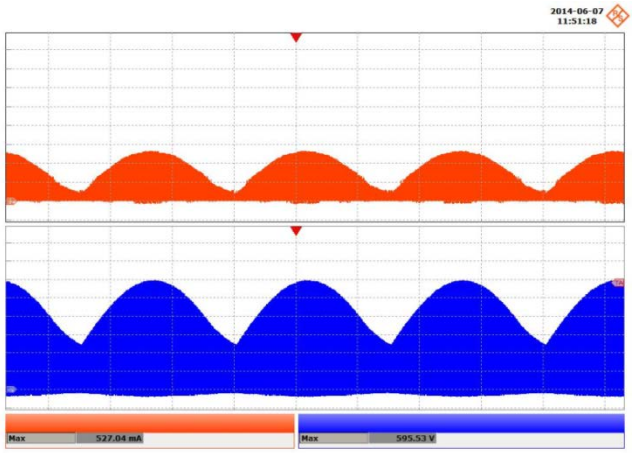

Figure 39 – 265 VAC, 50 Hz.
Upper: I_{DRAIN}, 0.2 A / div.
Lower: V_{DRAIN}, 100 V, 5 ms / div.

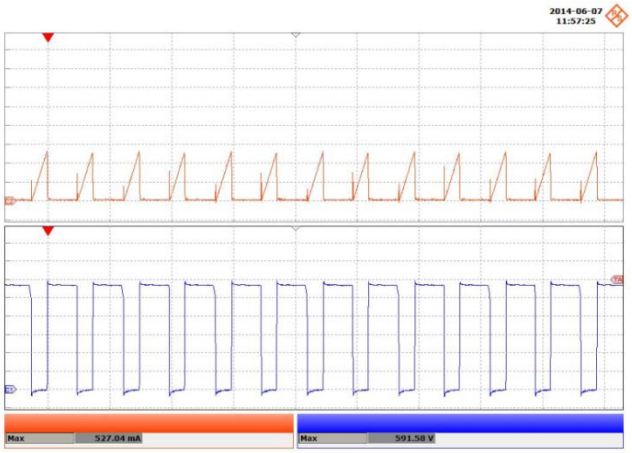

Figure 40 – 265 VAC, 50 Hz.
Upper: I_{DRAIN}, 0.2 A / div.
Lower: V_{DRAIN}, 100 V / div., 10 μs / div.

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11.5 Start-up Drain Voltage and Current

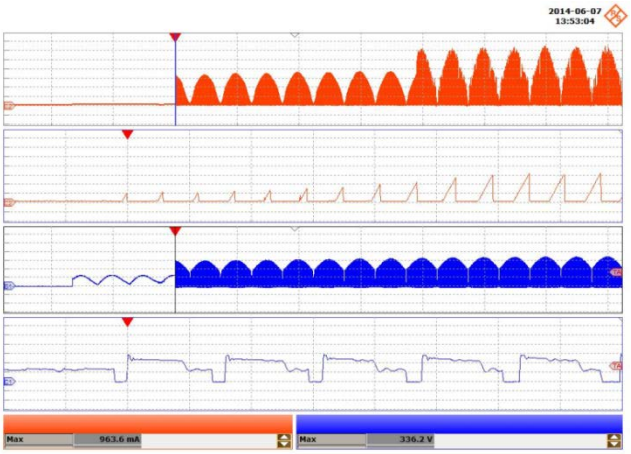

Figure 41 – 90 VAC, 50 Hz Start-up.
Upper: I_{DRAIN}, 0.2 A / div.
Lower: V_{DRAIN}, 100 V, 20 ms / div.

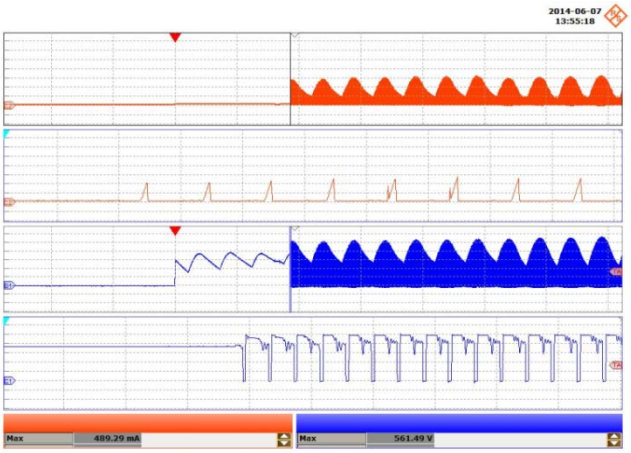

Figure 42 – 265 VAC, 50 Hz Start-up.
Upper: I_{DRAIN}, 0.2 A / div.
Lower: V_{DRAIN}, 100 V, 20 ms / div.

11.6 Drain Current and Drain Voltage During Output Short Condition

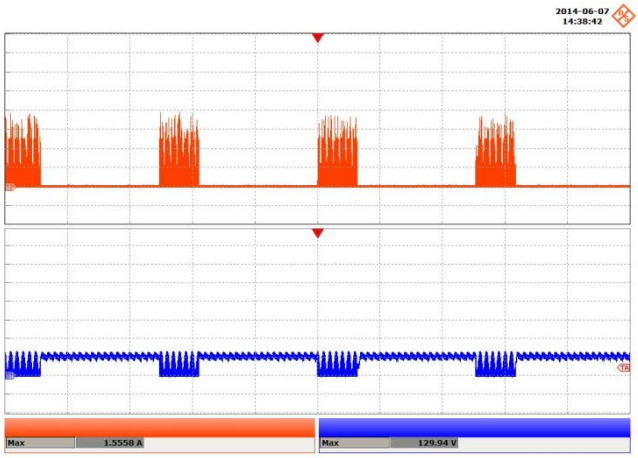

Figure 43 – 90 VAC, 50 Hz Output Short Condition.
Upper: I_{DRAIN}, 400 mA / div.
Lower: V_{DRAIN}, 100 V, 100 ms / div.

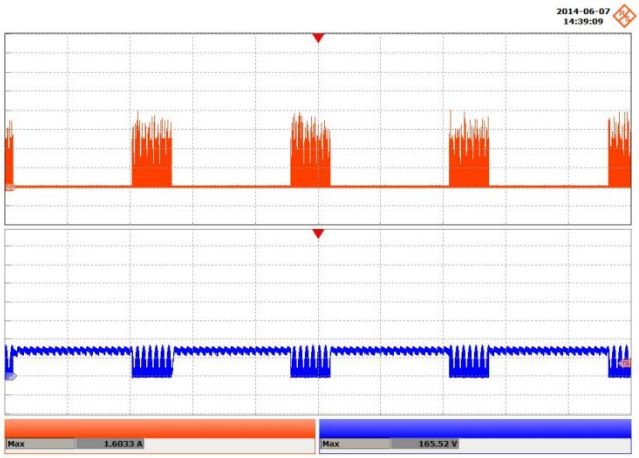

Figure 44 – 115 VAC, 50 Hz Output Short Condition.
Upper: I_{DRAIN}, 400 mA / div.
Lower: V_{DRAIN}, 100 V, 100 ms / div.

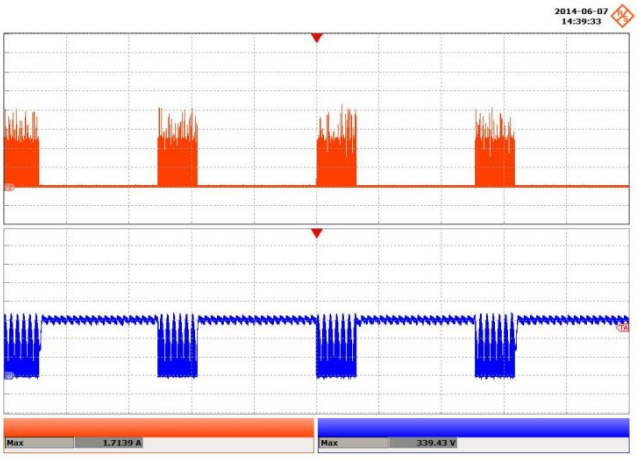

Figure 45 – 230 VAC, 50 Hz Output Short Condition.
Upper: I_{DRAIN}, 400 mA / div.
Lower: $V_{DRAIN,}$ 100 V, 100 ms / div.

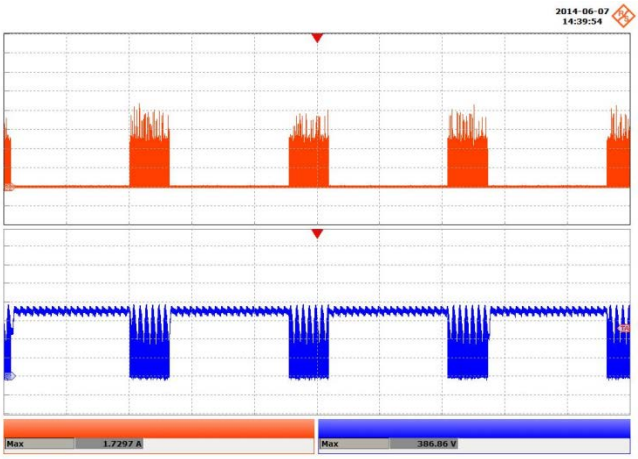

Figure 46 – 265 VAC, 50 Hz Output Short Condition.
Upper: I_{DRAIN}, 400 mA / div.
Lower: $V_{DRAIN,}$ 100 V, 100 ms / div.

11.7 Open Load Characteristic

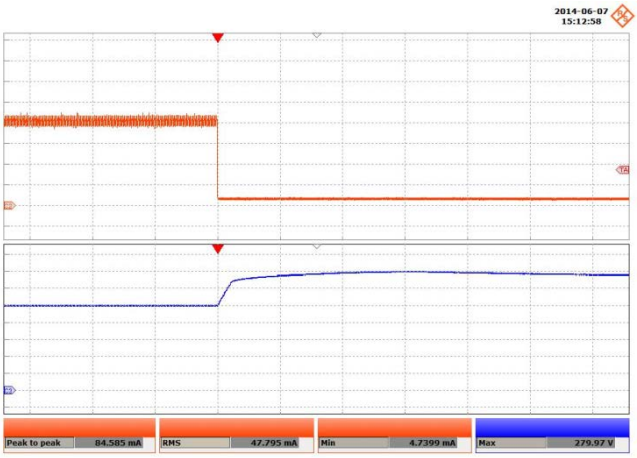

Figure 47 – 115 VAC, 50 Hz Running Open Load.
Upper: I_{OUT}, 20 mA / div.
Lower: V_{OUT}, 40 V / div., 400 ms / div.

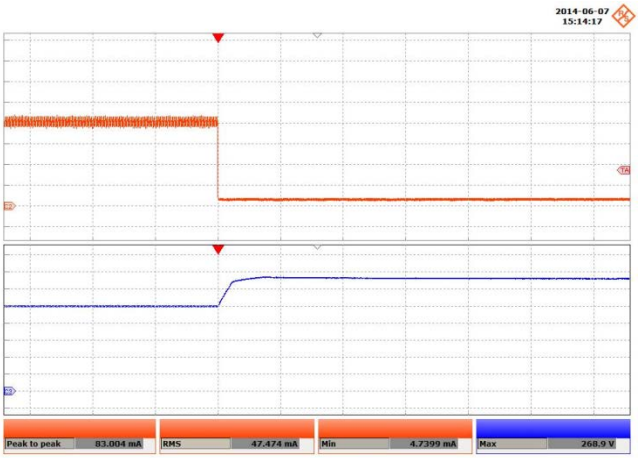

Figure 48 – 230 VAC, 50 Hz Running Open Load.
Upper: I_{OUT}, 20 mA / div.
Lower: V_{OUT}, 200 V / div., 400 ms / div.

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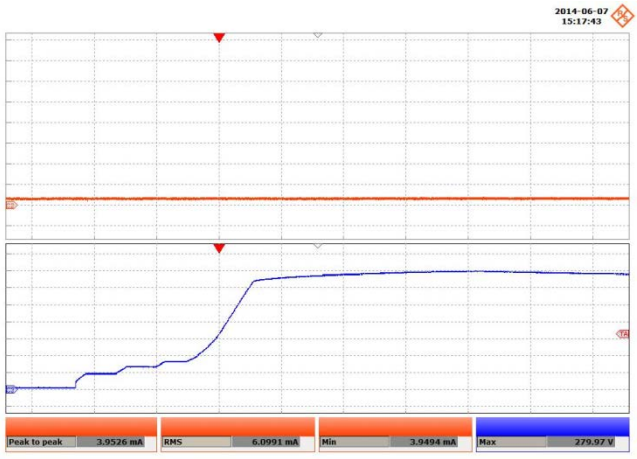

Figure 49 – 115 VAC, 50 Hz Open Load Start-up.
Upper: I_{OUT}, 20 mA / div.
Lower: V_{OUT}, 40 V / div., 400 ms / div.

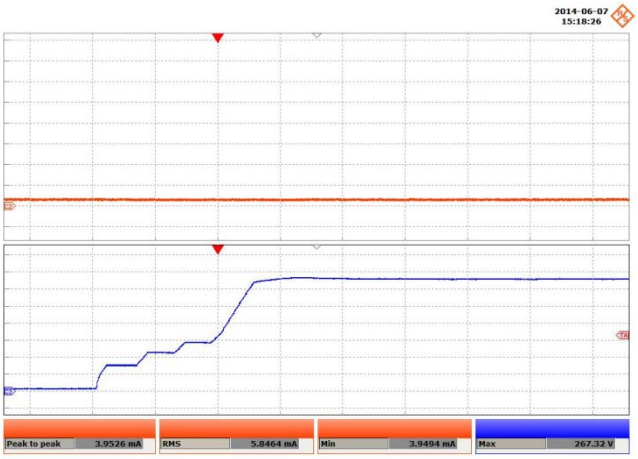

Figure 50 – 230 VAC, 50 Hz Open Load Start-up.
Upper: I_{OUT}, 20 mA / div.
Lower: V_{OUT}, 40 V / div., 400 ms / div.

12 Conducted EMI

12.1 Test Set-up

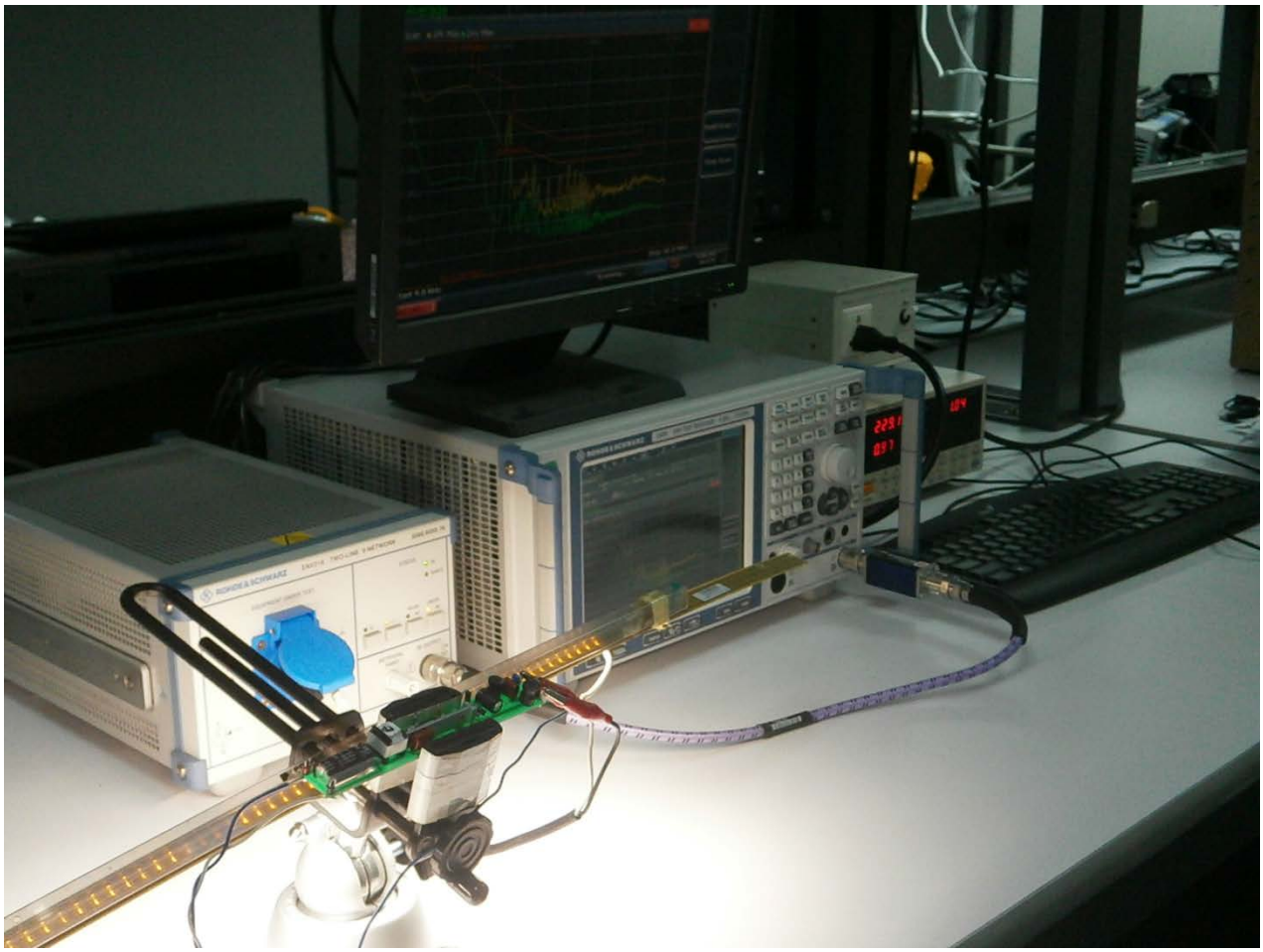

Figure 51 – Conducted EMI Test Set-up.

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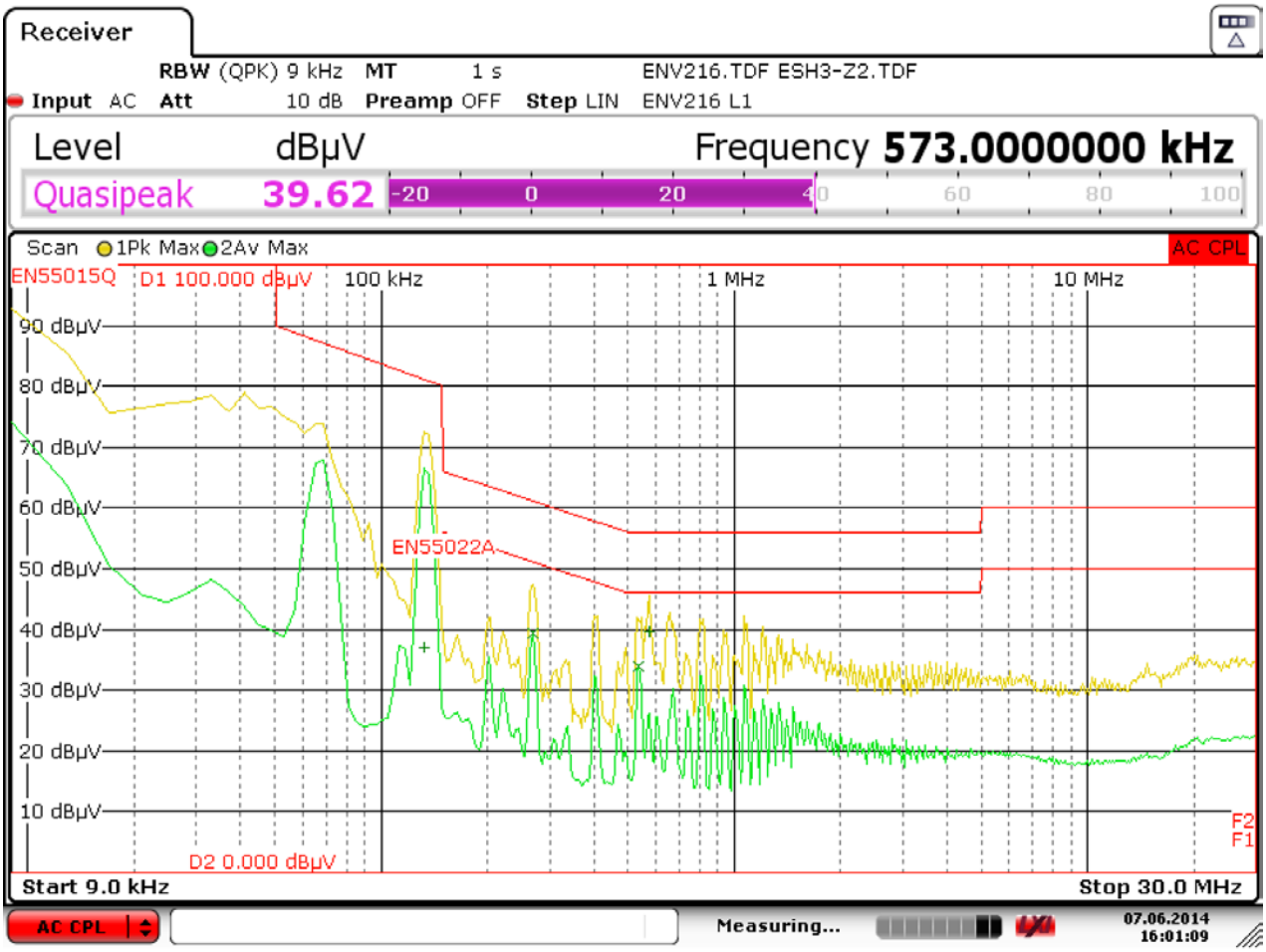
12.2 115 VAC Test Result



Date: 7.JUN.2014 16:01:08

Figure 52 – Conducted EMI, ~200 V LED Load, 115 VAC, 60 Hz, and EN55015 B Limits.

Trace1: EN55015Q **Trace2: EN55022A**

Trace/Detector	Frequency	Level dBµV	DeltaLimit
2 Average	269.0000 kHz	39.33 L1	-11.82 dB
2 Average	537.0000 kHz	34.03 L1	-11.97 dB
1 Quasi Peak	573.0000 kHz	39.62 L1	-16.38 dB
1 Quasi Peak	133.0000 kHz	37.09 L1	-44.00 dB

Figure 53 – Conducted EMI, Final Measurement Results.

12.3 230 VAC Test Result

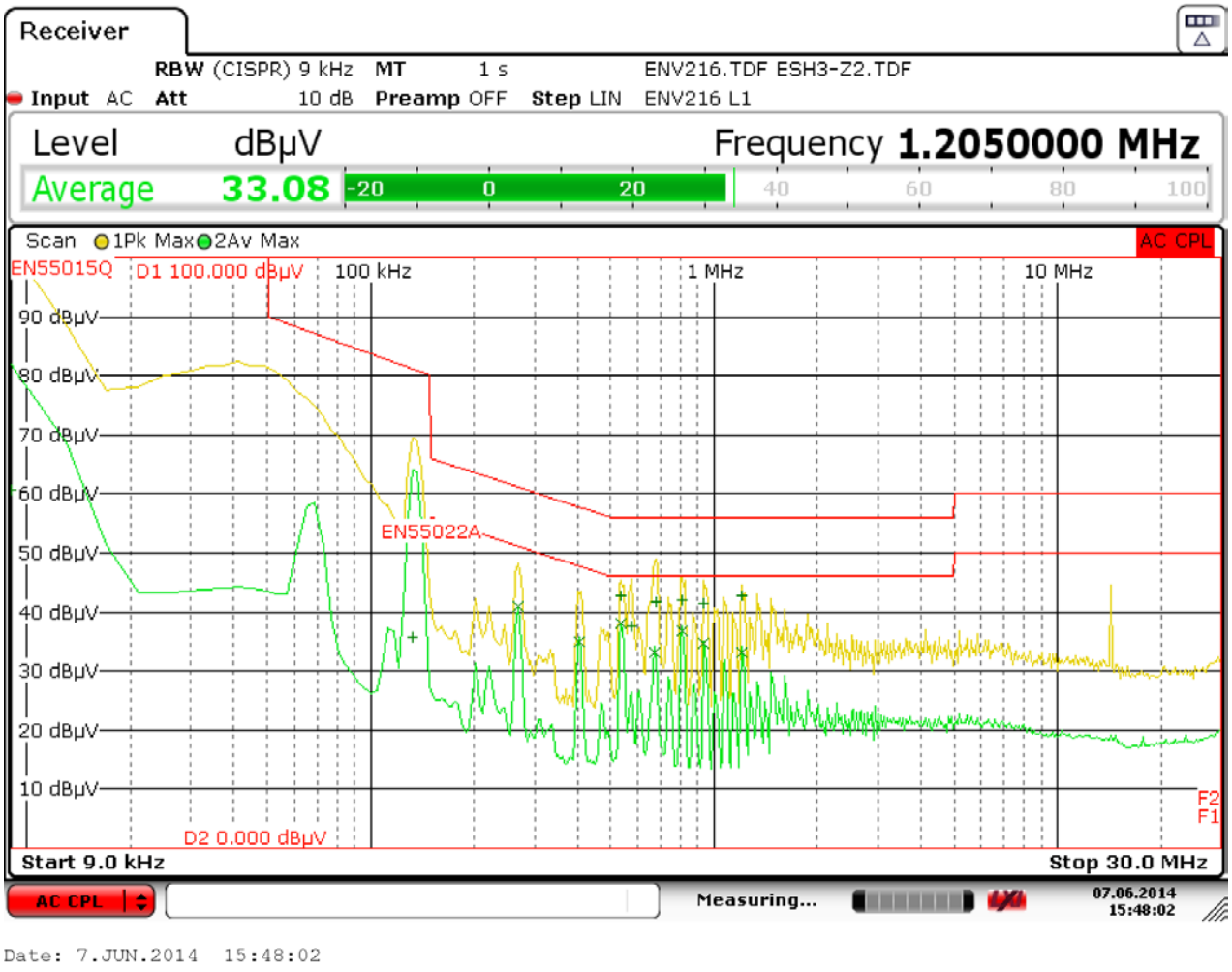


Figure 54 – Conducted EMI, ~200 V LED Load, 230 VAC, 60 Hz, and EN55015 B Limits.

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Trace/Detector	Frequency	Level dBµV	DeltaLimit
2 Average	537.0000 kHz	38.04 L1	-7.96 dB
2 Average	805.0000 kHz	36.73 N	-9.27 dB
2 Average	269.0000 kHz	40.81 N	-10.34 dB
2 Average	937.0000 kHz	34.64 N	-11.36 dB
2 Average	673.0000 kHz	33.23 N	-12.77 dB
2 Average	405.0000 kHz	34.93 L1	-12.82 dB
2 Average	1.2050 MHz	33.10 N	-12.90 dB
1 Quasi Peak	537.0000 kHz	42.82 L1	-13.18 dB
1 Quasi Peak	1.2010 MHz	42.63 L1	-13.37 dB
1 Quasi Peak	805.0000 kHz	42.01 L1	-13.99 dB
1 Quasi Peak	681.0000 kHz	41.76 L1	-14.24 dB

Figure 55 – Conducted EMI, Final Measurement Results.

13 Line Surge

The unit was subjected to ±2500 V, 100 kHz ring wave and ±1000 V differential surge using 10 strikes for each condition. A test failure was defined as a non-recoverable interruption of output requiring either repair or recycling of input voltage.

13.1 Test Results

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+1000	115	L to N	90	Pass
-1000	115	L to N	90	Pass
+1000	115	L to N	0	Pass
-1000	115	L to N	0	Pass

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+1000	230	L to N	90	Pass
-1000	230	L to N	90	Pass
+1000	230	L to N	0	Pass
-1000	230	L to N	0	Pass

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+2500	115	L to N	90	Pass
-2500	115	L to N	90	Pass
+2500	115	L to N	0	Pass
-2500	115	L to N	0	Pass

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+2500	230	L to N	90	Pass
-2500	230	L to N	90	Pass
+2500	230	L to N	0	Pass
-2500	230	L to N	0	Pass

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13.2 Surge Drain Waveforms

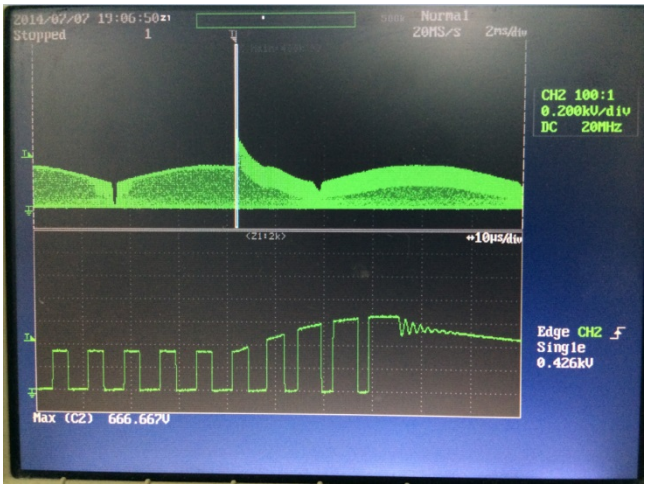

Figure 56 – 115 VAC, +1 kV Differential Surge, 90° V_{DRAIN}, 200 V / div., 2 ms / div.

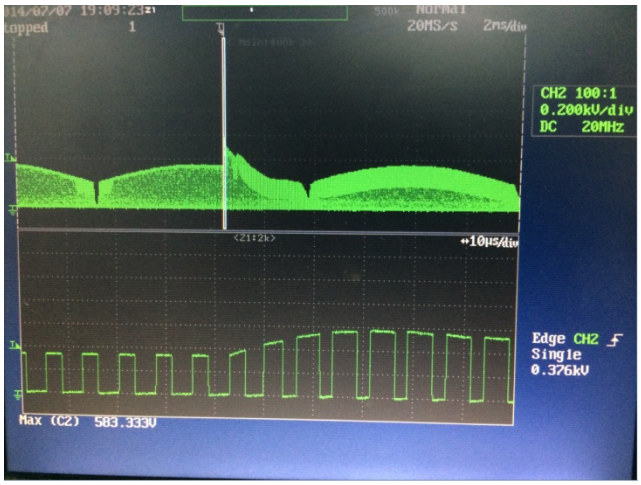

Figure 57 – 115 VAC, -1 kV Differential Surge, 90° V_{DRAIN}, 200 V / div., 2 ms / div.

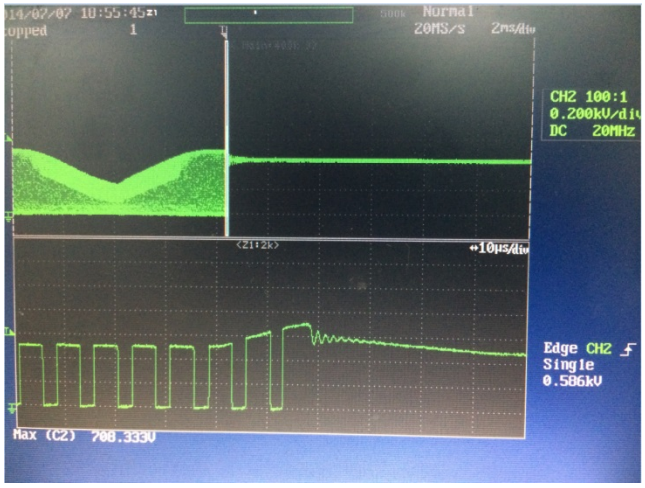

Figure 58 – 230 VAC, +1 kV Differential Surge, 90° V_{DRAIN}, 200 V / div., 2 ms / div.

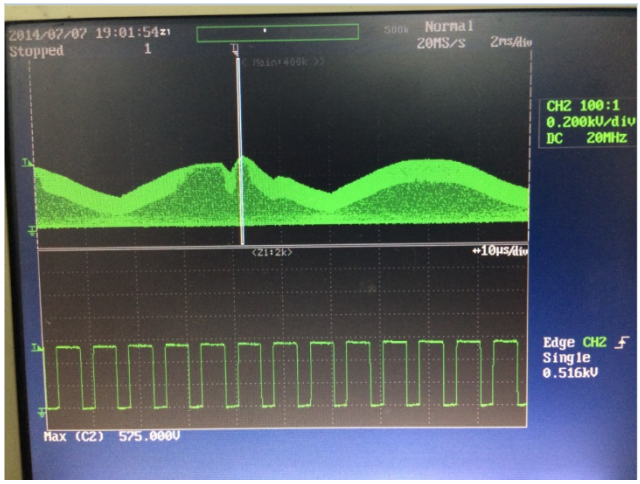

Figure 59 – 230 VAC, -1 kV Differential Surge, 90° V_{DRAIN}, 200 V / div., 2 ms / div.

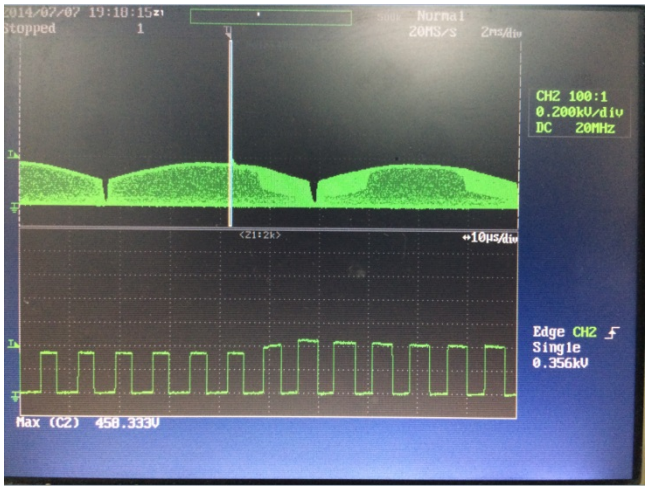

Figure 60 – 115 VAC, +2.5 kV Ring Wave Surge, 90° V_{DRAIN}, 200 V / div., 2 ms / div.

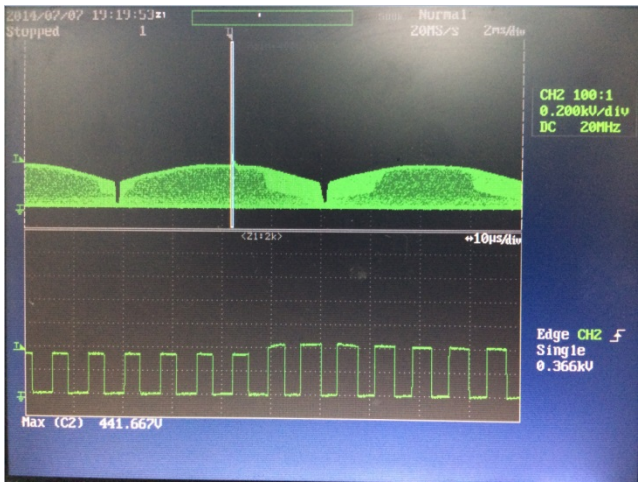

Figure 61 – 115 VAC, -2.5 kV Ring Wave Surge, 90° V_{DRAIN}, 200 V / div., 2 ms / div.

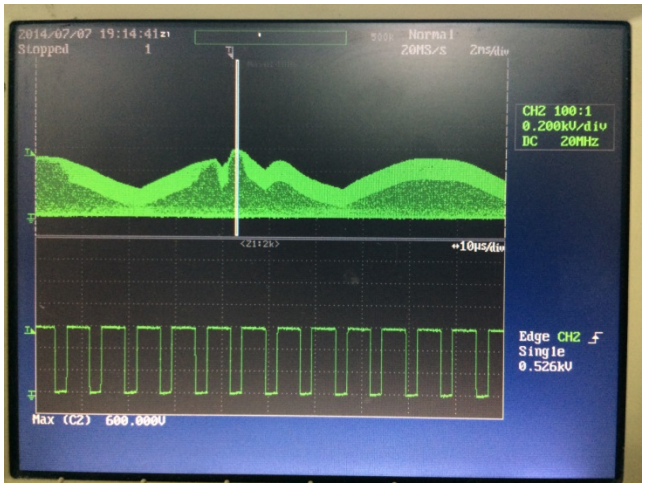

Figure 62 – 230 VAC, +2.5 kV Ring Wave Surge, 90° V_{DRAIN}, 200 V / div., 2 ms / div.

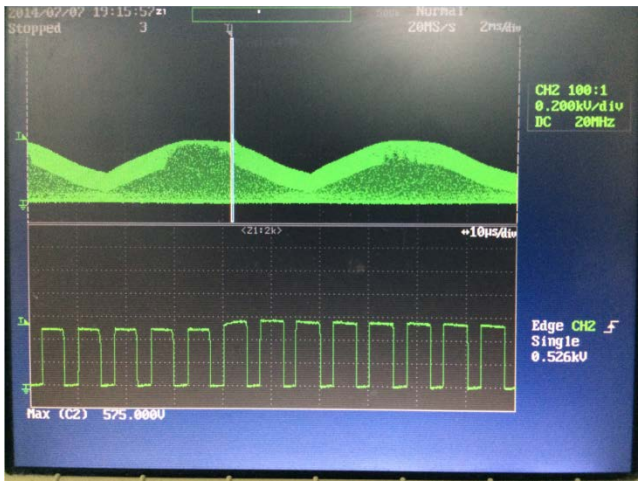

Figure 63 – 230 VAC, -2.5 kV Ring Wave Surge, 90° V_{DRAIN}, 200 V / div., 2 ms / div.

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14 Appendix: Using LYTSwitch-4 Low Line Device for Universal Input in Buck-Boost Configuration

LYTSwitch-4 Low Line family devices are intended for single low line input operation however, it may be used for universal input operation. The following guidelines are provided for a universal input design.

Step by Step Procedure for Setting Output Current

Step 1: For Buck-Boost configuration use LYTSwitch-4 High Line Flyback PIXIs by setting VOR [39] = VO [7]. Enter other desired values for VACMAX [B], IO [B], n [B], and KP [B].

1	ACDC_LYTSwitch-4_010614; Rev.1.4; Copyright Power Integrations 2014	INPUT	INFO	OUTPUT	UNIT	LYTSwitch-4_010614: Flyback Transformer Design Spreadsheet
2	ENTER APPLICATION VARIABLES					Design Title
3	Dimming required	NO		NO		Select 'YES' option if dimming is required. Otherwise select 'NO'.
4	VACMIN	90		90	V	Minimum AC Input Voltage
5	VACMAX	265		265	V	Maximum AC input voltage
6	fL			60	Hz	AC Mains Frequency
7	VO	200.00		200	V	Typical output voltage of LED string at full load
8	VO_MAX			220.00	V	Maximum expected LED string Voltage.
9	VO_MIN			180.00	V	Minimum expected LED string Voltage.
10	V_OVP			242.00	V	Over-voltage protection setpoint
11	IO	0.075		0.08	A	Typical full load LED current
12	PO			15.0	W	Output Power
13	n	0.870		0.87		Estimated efficiency of operation
14	VB			20	V	Bias Voltage
15						
16						

Figure 64 – PIXIs Spreadsheet Showing Input Cells.

1	ACDC_LYTSwitch-4_010614; Rev.1.4; Copyright Power Integrations 2014	INPUT	INFO	OUTPUT	UNIT	LYTSwitch-4_010614: Flyback Transformer Design Spreadsheet
36	Key Design Parameters					
37	KP	0.80		0.80		Ripple to Peak Current Ratio (For PF > 0.9, 0.4 < KP < 0.9)
38	LP			1694	uH	Primary Inductance
39	VOR	200.00		200	V	Reflected Output Voltage.
40	Expected IO (average)			0.07	A	Expected Average Output Current
41	KP_VACNOM			0.76		Expected ripple current ratio at VACNOM (115VAC)
42	TON_MIN			1.66	us	Minimum on time at maximum AC input voltage
43	PCLAMP			0.11	W	Estimated dissipation in primary clamp
44						

Figure 65 – PIXIs Spreadsheet Showing KP and VOR Values.

Step 2: Use 3.6 MΩ resistor as initial value for upper RV [B] V pin resistor, this is the recommended value for high line application and use the FB feedback pin resistor value in RFB1 [C] as calculated by PIXIs. This first assumption will provide output current close to the desired output. Expect that output current will be much higher at high line input. This will be corrected in later steps. Choose Auto for LYTSwitch-4 [D] device selection cell and REDuce for Current Limit Mode [20]. Adjust I_{FB} [29] until Expected IO (average) [D] becomes almost equals to the specified IO [B] output current. Use Goal Seek for faster results.

1	ACDC_LYTSwitch-4_010614; Rev.1.4; Copyright Power Integrations 2014	INPUT	INFO	OUTPUT	UNIT	LYTSwitch-4_010614: Flyback Transformer Design Spreadsheet
17	ENTER LYTSwitch-4 VARIABLES					
18	LYTSwitch-4	Auto		LYT4213		Selected LYTSwitch-4
19						
20	Current Limit Mode	RED		RED		Select "RED" for reduced Current Limit mode or "FULL" for Full current limit mode
21	ILIMITMIN			1.00	A	Minimum current limit
22	ILIMITMAX			1.16	A	Maximum current limit
23	fS			132000	Hz	Switching Frequency
24	fSmin			124000	Hz	Minimum Switching Frequency
25	fSmax			140000	Hz	Maximum Switching Frequency
26	IV			44.3	uA	V pin current
27	RV	3.60		3.6	M-ohms	Upper V pin resistor
28	RV2			1E+12	M-ohms	Lower V pin resistor
29	IFB	131.75		131.75	uA	FB pin current (85 uA < IFB < 210 uA)
30	RFB1			129.0	k-ohms	FB pin resistor
31	VDS			10	V	LYTSwitch on-state Drain to Source Voltage
32	VD			0.50	V	Output Winding Diode Forward Voltage Drop (0.5 V for Schottky and 0.8 V for PN diode)
33	VDB			0.70	V	Bias Winding Diode Forward Voltage Drop
34						
35						

Figure 66 – PIXls Spreadsheet Showing RV and RFB1 Values to be Used on the First Prototype Pass.

1	ACDC_LYTSwitch-4_010614; Rev.1.4; Copyright Power Integrations 2014	INPUT	INFO	OUTPUT	UNIT	LYTSwitch-4_010614: Flyback Transformer Design Spreadsheet
36	Key Design Parameters					
37	KP	0.80		0.80		Ripple to Peak Current Ratio (For PF > 0.9, 0.4 < KP < 0.9)
38	LP			1669	uH	Primary Inductance
39	VOR	200.00		200	V	Reflected Output Voltage.
40	Expected IO (average)			0.0751	A	Expected Average Output Current
41	KP_VACNOM			0.76		Expected ripple current ratio at VACNOM (115VAC)
42	TON_MIN			1.64	us	Minimum on time at maximum AC input voltage
43	PCLAMP			0.11	W	Estimated dissipation in primary clamp
44						

Figure 67 – PIXls Spreadsheet Showing Expected IO (Average) Cell.

Step 3: Fine tune the feedback resistor to provide correct output current at low line input and set nominal output current at nominal input voltage. Using data from Step 2 enter actual measurements in the cells under FB pin resistor Fine Tuning section - RFB1 [B], VB1 [B], IO1 [B] = IO2 [B], then use values from RFB1 (new) [D]. Repeat until desired target value is achieved. Again, output current maybe much higher at high line input but this will be corrected in the next step.

1	ACDC_LYTSwitch-4_010614; Rev.1.4; Copyright Power Integrations 2014	INPUT	INFO	OUTPUT	UNIT	LYTSwitch-4_010614: Flyback Transformer Design Spreadsheet
119	FB pin resistor Fine Tuning					
120	RFB1	182.00		182	k-ohms	Upper FB Pin Resistor Value
121	RFB2			1E+12	k-ohms	Lower FB Pin Resistor Value
122	VB1	21.00		21.0	V	Test Bias Voltage Condition1
123	VB2			22.1	V	Test Bias Voltage Condition2
124	IO1	0.0750		0.0750	A	Measured Output Current at Vb1
125	IO2	0.0750		0.0750	A	Measured Output Current at Vb2
126	RFB1 (new)			182.0	k-ohms	New RFB1
127	RFB2(new)			1.00E+12	k-ohms	New RFB2
128						
129						

Figure 68 – PIXls Spreadsheet Showing Input Cells for FB Pin Resistor Fine Tuning.

Step 4: Employ FB Offset Circuit shown in Figure 4 in Section 4.6 by connecting R16 to FB pin of LYTSwitch-4, find the value of R16, start at 500 kΩ then reduce the value until the output current at 230 VAC is almost equal to the 115 VAC as initially set in Step 3.

Step 5: The objective in this step is not to get to exactly the desired output current but to make the line regulation flat across the entire input range. Use the Fine Tuning section for upper (RV1) and (RV2) lower V pin resistors to optimize regulation across the entire

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input range. Enter 3.6 MΩ resistor to RV1 [B] as originally used in Step 2 and enter 1.1 MΩ value for RV2 [B] V-pin resistor. Enter measured output currents at VAC1 [D] and VAC2 [D] in IO_VAC1 [B] and IO_VAC2 respectively. Replace V pin resistors with the new V pin resistors RV1 (new) [D] and RV2 (new) [D] as calculated by PIXls and re-measure output.

Repeat the process until measured output currents at VAC1 [D] and VAC2 [D] are almost equal then repeat Step 3 to get desired output current set at IO [B] in step 1.

1	ACDC_LYTSwitch-4_010614; Rev.1.4; Copyright Power Integrations 2014	INPUT	INFO	OUTPUT	UNIT	LYTSwitch-4_010614: Flyback Transformer Design Spreadsheet
106	FINE TUNING (Enter measured values from prototype)					
107	V pin Resistor Fine Tuning					
108	RV1	3.60		3.60	M-ohms	Upper V Pin Resistor Value
109	RV2	1.10		1.1	M-ohms	Lower V Pin Resistor Value
110	VAC1			115.0	V	Test Input Voltage Condition1
111	VAC2			230.0	V	Test Input Voltage Condition2
112	IO_VAC1	0.0750		0.0750	A	Measured Output Current at VAC1
113	IO_VAC2	0.0750		0.0750	A	Measured Output Current at VAC2
114	RV1 (new)			3.60	M-ohms	New RV1
115	RV2 (new)			1.10	M-ohms	New RV2
116	V_OV			294.8	V	Typical AC input voltage at which OV shutdown will be triggered
117	V_UV			66.9	V	Typical AC input voltage beyond which power supply can startup
118						

Figure 69 – PIXls Spreadsheet Showing Input Cells for V Pin Resistor Fine Tuning.

15 Revision History

Date	Author	Revision	Description and Changes	Reviewed
11-Mar-15	AM	1.0	Initial Release	Apps & Mktg

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