

Two and four-quadrant DC/DC converters with SCALE drivers

Notes for the use of dead-time logic

by Heinz Rüedi, CT-Concept Technology Ltd. Switzerland

Introduction

Whereas the most widely used DC/DC converter topologies operate only in single-quadrant mode, a 2 or 4-quadrant control range is required in some applications. These include DC/DC converters which can transport energy in both forwards and reverse directions as well as buck/boost converters. Figure 1 illustrates the basic circuit of a 2-quadrant buck converter.

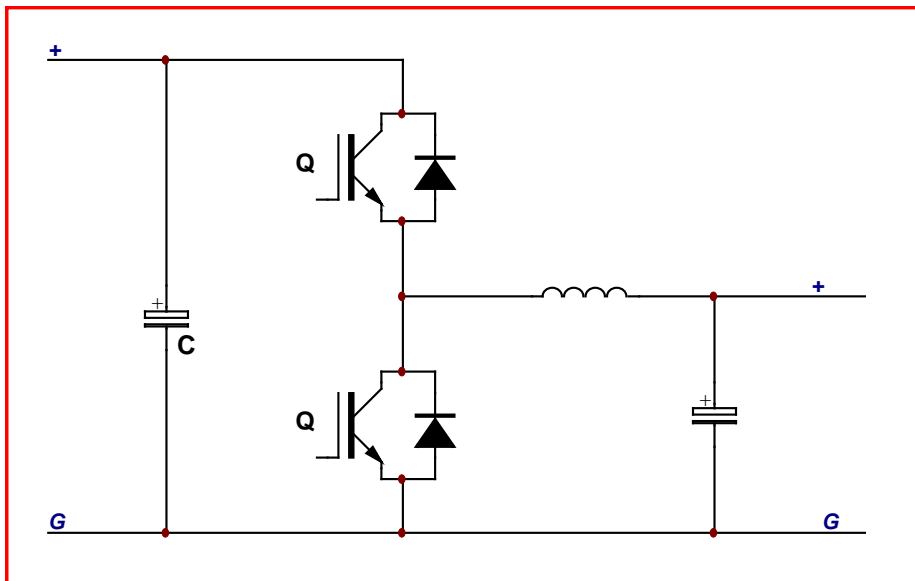


Fig. 1 Two-quadrant buck converter

Application Note

The circuit can be rotated to obtain a 2-quadrant up-converter. Only one switch is clocked, depending on the desired direction of energy flow. The opposite transistor in each case has no importance as only the freewheeling diode is used. The two switches Q1 and Q2 must never conduct simultaneously; provision must be made for a dead time when changing over between Q1 and Q2.

Use of SCALE drivers

SCALE drivers are also ideal for applications of this kind. Firstly in the normal way where both transistors are always operated in half-bridge configuration, so that the SCALE driver (in half-bridge mode) can also generate the required dead times.

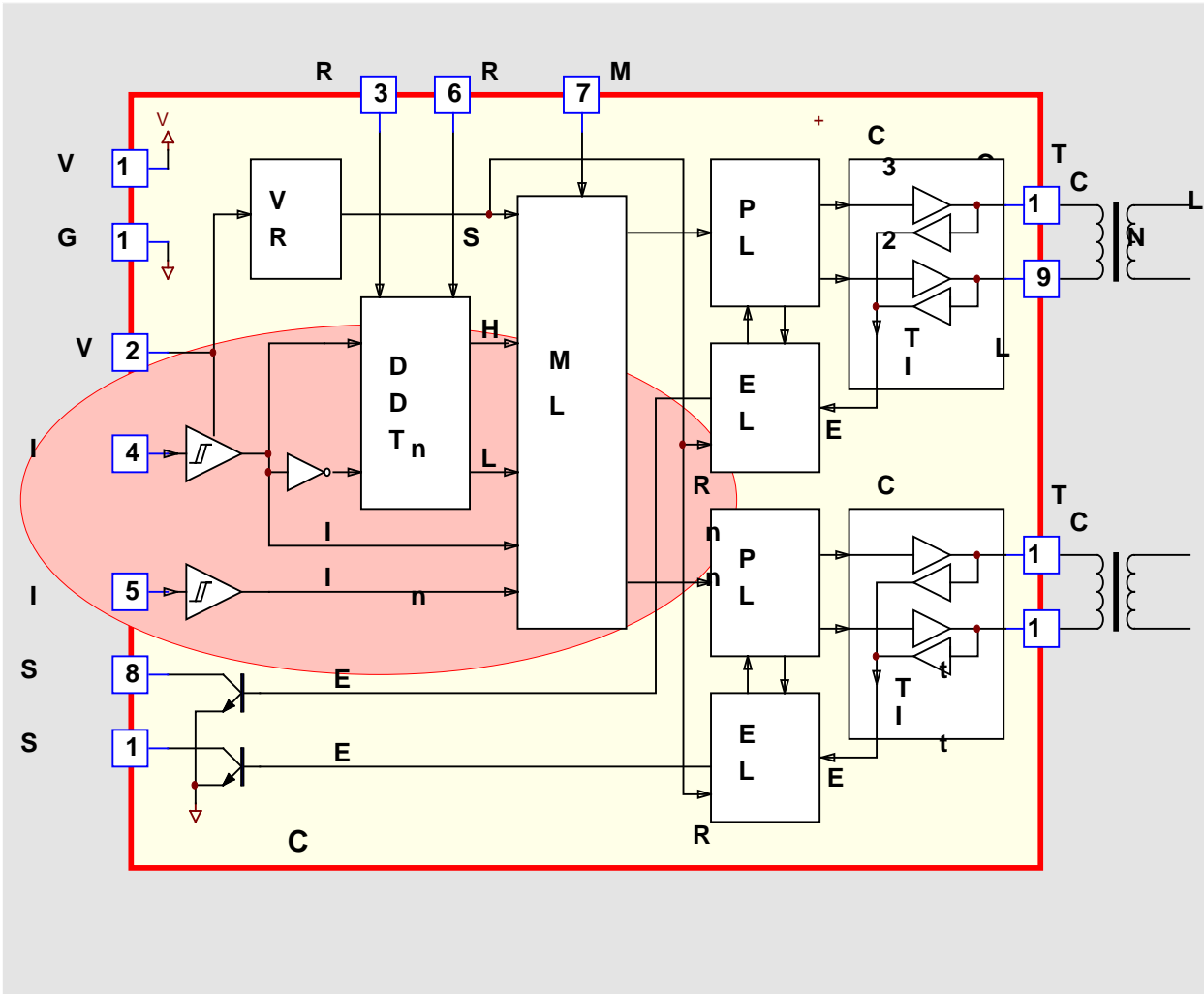


Fig. 2 Block diagram of the LDI 001 logic-to-driver interface

Application Note

If only Q1 or Q2 are to be clocked depending on the desired direction of energy flow, the driver's direct mode can be used. The controller must then prevent both transistors from conducting simultaneously and must ensure that a specific dead time is maintained when changing over between Q1 and Q2 and vice-versa.

But there is also an easier way – by looking more closely at the inside of the circuit.

The input signals are processed in the LDI 001 (an ASIC used in the SCALE driver). However, the block diagram of this ASIC (Fig. 2) does not reveal any details of how the signals are actually processed.

Figure 3 shows the signal processing in half-bridge mode. The signal applied to input A is fed to the dead-time circuits – once inverted and once not. An AND gate is located behind the input; both outputs can be deactivated with input B.

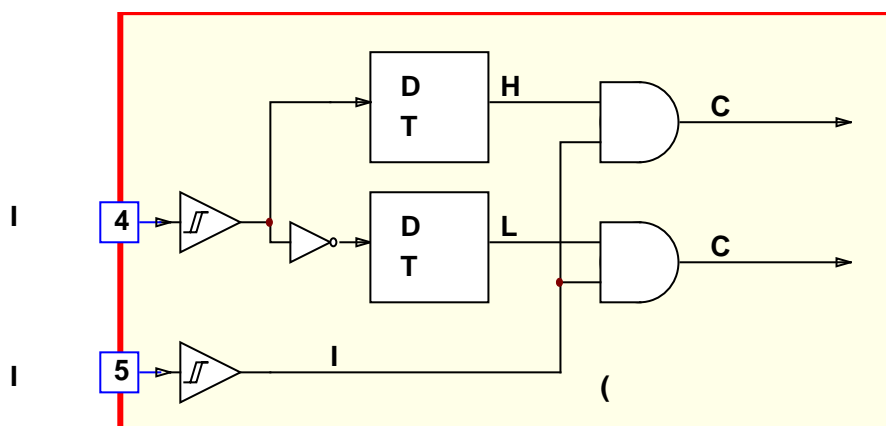


Fig. 3 Circuit principle in half-bridge mode

If the information about the direction of energy flow is applied to input A and the PWM signal to input B, then the required characteristic is obtained with no additional circuits:

- : Either Q1 or Q2 can be used for clocking, the opposite switch is always blocked. The driver applies the PWM signal present at input B in undistorted form (without adding a dead time) to the corresponding power switch.
- : Whenever switchover takes place between Q1 and Q2 and vice-versa, the driver generates a dead time.

Application Note

Figure 4 shows the resulting signal profile.

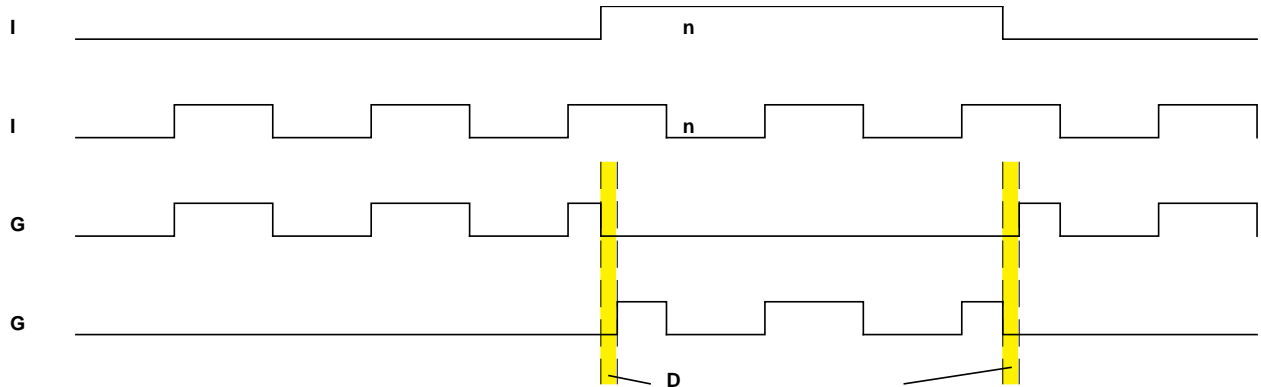


Fig. 4 Signal profiles in the application

Supplementary notes

We take great care in preparing our application notes. However, we cannot guarantee that the circuits and procedures shown will operate without problems in every application. This must be established by the user himself. Neither can we guarantee that the suggestions are free of third-party rights.

Manufacturer

Your Distribution Partner

CT-Concept Technology Ltd.
 Intelligent Power Electronics
 Hauptstrasse 3
 CH-2533 Leubringen / Evilard
 (Switzerland)

Tel ++41 (0)32 / 322 42 36
 Fax ++41 (0)32 / 322 22 51
 E-Mail info@ct-concept.com
 Internet www.CT-CONCEPT.com
 Internet www.IGBT-Driver.com

Application Note

© Copyright 1997...1999 by CT-Concept Technology Ltd. - Switzerland.
We reserve the right to make any technical modifications without prior notice.

All rights reserved.
Version from 14.04.16