General Purpose Base Board for SCALE-iDriver™ SIC1182K

<table>
<thead>
<tr>
<th>Application</th>
<th>General purpose drives, UPS, PV power and others</th>
</tr>
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</table>
| Specification                | • Suitable for Half-bridge SiC-MOSFET power modules in 62mm housing  
                                • Up to 800V DC-link voltage  
                                • Electrical Interface  
                                • Short Circuit Detection  
                                • Advanced Active Clamping  
                                • Source-Controller |

<table>
<thead>
<tr>
<th>Author</th>
<th>Application Engineering Gate Drivers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Document Number</td>
<td>RDHP-1901</td>
</tr>
<tr>
<td>Revision¹</td>
<td>A.2</td>
</tr>
</tbody>
</table>

¹ The letter refers to the hardware revision. The number refers to the documentation revision.
**Scope**

This application proposal provides a circuit design for a general purpose base board for driving various SiC-MOSFET power modules.

Main features of the design are:

- Suitable for SiC-MOSFET power modules in 62mm housing with a maximum blocking voltage of 1200 V
- Two channels for half-bridge modules
- Short Circuit Detection
- Advanced Active Clamping
- Electrical command inputs and status outputs
- 0 V/5 V command input logic
- 0 V/5 V status output logic
- Minimum pulse suppression
- 5 V supply voltage
- Single PCB solution with soldered-in gate driver IC
- Adjustable Source Controller

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**Application Conditions**

The design is proposed for the following application conditions:

- general purpose applications
- SiC-MOSFET power modules
- Up to 8A peak current
- Up to 1.3 W per channel
- Ambient Temperature: -40... 85°C
Design Description

In addition to the following design description, reference to datasheet of the gate driver SIC1182K is recommended.

Equivalent Circuit

As an overview the equivalent circuit of the design RDHP-1901 is shown in Figure 1.

Figure 1: Equivalent Circuit of RDHP-1901
**Gate Resistors**

Gate resistor values are not explicitly given as they depend on the power module used and on the application. Gate resistors of SMD (size 1206) package can be selected. Their position is depicted in Figure 2.

<table>
<thead>
<tr>
<th>Turn-On Gate Resistors</th>
<th>Turn-Off Gate Resistors</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel</td>
<td>SMD Package</td>
</tr>
<tr>
<td>1</td>
<td>R113a ... R113d</td>
</tr>
<tr>
<td>2</td>
<td>R213a ... R213d</td>
</tr>
</tbody>
</table>

The gate resistors must be determined and assembled by the user.

![Figure 2: Position of Gate Resistors](https://gate-driver.power.com/ Page4)
Short Circuit Detection

The SIC1182K gate driver IC from Power Integrations provides a sense input for monitoring short-circuit conditions of the power semiconductor. This design offers a short circuit detection function using a resistor network. A assembly variant of implementation tested with Wolfspeed CAS300M12BM2 is described in the following table:

<table>
<thead>
<tr>
<th>Channel</th>
<th>Resistor Chain</th>
<th>Timing Resistor</th>
<th>Timing Capacitor</th>
<th>Decoupling Resistor</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>R100 ... R108</td>
<td>R109</td>
<td>C100</td>
<td>R110</td>
</tr>
<tr>
<td></td>
<td>270 kΩ each</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>R200 ... R208</td>
<td>R209</td>
<td>C200</td>
<td>R210</td>
</tr>
<tr>
<td></td>
<td>270 kΩ each</td>
<td></td>
<td></td>
<td>3.3 kΩ</td>
</tr>
</tbody>
</table>

All mentioned components as shown in Figure 3 can be changed to meet the desired behavior of the short circuit detection.

- R100 ... R108 and R200 ... R208 are dimensioned for 1200 V power semiconductors and can be decreased according to data sheet of SIC1182K when using lower voltage ranges.
- Increasing R109 and R209 accelerates the SC detection time and lowers the detection threshold voltage.
- Increasing C100 and C200 increases the short circuit detection time but avoids false tripping and weakens the Active Clamping efficiency if implemented.
- Decreasing R110 and R210 helps to avoid false tripping of the short circuit detection.

The details of the short circuit detection function are described in the corresponding data sheet of the gate driver.

Figure 3: Position of components for Short Circuit Detection
Advanced Active Clamping

Active clamping is a technique designed to partially turn on the power semiconductor in case the voltage across the device exceeds a predefined threshold. The power semiconductor is then kept in linear operation. Basic active clamping topologies implement a single feedback path from the Collector/Drain through transient voltage suppressor (TVS) diodes to the gate. This design proposal supports Power Integrations Advanced Active Clamping realized by the SNS pin of the SIC1182K based on the following principle.

When active clamping is activated, the turn-off MOSFET of the gate driver is switched off in order to improve the effectiveness of the active clamping and to reduce the losses in the TVS diodes. At the same time the turn-on MOSFET of the SIC1182K is supplying (additionally to the TVS diodes) a controlled gate current to keep the power semiconductor in the active region. This feature called Advanced Active Clamping is mainly integrated in the secondary side of the SIC1182K.

A assembly variant as shown in Figure 4 of implementation tested with Wolfspeed CAS300M12BM2 is described in the following table:

<table>
<thead>
<tr>
<th>Channel (x)</th>
<th>TVS Chain</th>
<th>TVS, bidirectional</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 and 2</td>
<td>Dx01 ... Dx05</td>
<td>Dx06</td>
</tr>
<tr>
<td></td>
<td>Littefuse P6SMB150A-E3</td>
<td>Vishay P6SMB150CA</td>
</tr>
</tbody>
</table>

Here the theoretical voltage limitation level is set to 900 V for a power semiconductor in the 1200 V-class. This value has to be changed accordingly when lower voltage classes are used.

![Figure 4: Position of components for Advanced Active Clamping](https://gate-driver.power.com/)
**Minimum Pulse Suppression**

This design possesses a minimum pulse suppression with a time constant $\tau$ of typically 99 ns. If required the setting can be changed by adjusting C300 and C306 which are depicted in Figure 5. The time constants are given by the following equations.

$$\tau_1 = 99 \, \Omega \cdot C300$$

$$\tau_2 = 99 \, \Omega \cdot C306$$

Recommended values of C300 and C306 are in the range of 1 nF ($\tau_x = 99$ ns) to 3.3 nF ($\tau_x = 327$ ns), depending on the actual application conditions.

![Figure 5: Position of Capacitors for the Minimum Pulse Suppression](image)

**Blocking Time**

During the blocking time, which is set to typically 10 $\mu$s, the SIC1182K ignores incoming command signals. The blocking time starts once a fault was detected by the gate driver IC’s secondary side (undervoltage lock-out or a short-circuit event) or when an undervoltage condition ends on the primary side.

For further details refer to the data sheet of the gate driver SIC1182K.
Source Controller
In order to realize the appropriate gate switching voltage levels an external source controller in addition to the SIC1182K is used. The following voltage levels are provided:

- Positive Rail (\(V_{VISO−Source}\)): 20 V (controlled)
- Negative Rail (\(V_{Source−COM}\)): -5 V (load dependent)

The positive rail is controlled by the help of a shunt regulator TL431BFDT by NXP. The regulated voltage is calculated with equation 3 using \(V_{ref} = 2495\, \text{mV}\) and \(I_{ref} = 2\, \mu\text{A}\).

\[
V_{VISO−Source} = V_{ref} \cdot \left(1 + \frac{R_{x16}}{R_{x17}}\right) + I_{ref} \cdot R_{x16}
\]  

(3)

In the proposed design the resistors like highlighted in Figure 6 are set to the following values:

- \(R_{x17} = 1.3\, \text{k}\Omega\)
- \(R_{x16} = 9.1\, \text{k}\Omega\)
- \(R_{x18} = 680\, \Omega\) (series resistor)

![Figure 6: Position of Capacitors for the Minimum Pulse Suppression](https://gate-driver.power.com/)
## Interfaces

The position of the interfaces of RDHP-1901 can be taken from Figure 7.

### Electrical Interfaces

<table>
<thead>
<tr>
<th>Pin</th>
<th>Designation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>V5</td>
<td>15 V-Power Supply (referenced to GND)</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>3</td>
<td>SO2</td>
<td>Status Output, Channel 2</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>5</td>
<td>INB</td>
<td>Command Input, Channel 2</td>
</tr>
<tr>
<td>6</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>7</td>
<td>SO1</td>
<td>Status Output, Channel 1</td>
</tr>
<tr>
<td>8</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>9</td>
<td>INA</td>
<td>Command Input, Channel 2</td>
</tr>
<tr>
<td>10</td>
<td>GND</td>
<td>Ground</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Pin</th>
<th>Designation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>G1</td>
<td>Gate of Top Switch</td>
</tr>
<tr>
<td>5</td>
<td>S1</td>
<td>Source of Top Switch</td>
</tr>
<tr>
<td>6</td>
<td>G2</td>
<td>Gate of Bottom Switch</td>
</tr>
<tr>
<td>7</td>
<td>S2</td>
<td>Source of Bottom Switch</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Pin</th>
<th>Designation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DC+</td>
<td>Drain/Collector of Top Switch, positive DC-Link Connection for 2-Level-Application</td>
</tr>
</tbody>
</table>
The set of CAD data, which includes the circuit schematics, Gerber files, assembly drawing, BOM and Pick-and-Place file are available as separate documents bundled together with this documentation.

**Layout Example**

![Layout Example Image](https://gate-driver.power.com/)

**Figure 8:** 3D-View on RDHP-1901
Figure 9: Assembly Drawing of RDHP-1901
Switching Characteristics

Turn-On and Turn-Off Behavior

The measurement examples shown with the SiC power module Wolfspeed CAS300M12BM2 ($R_{G,ON} = 2.5 \, \Omega$ and $R_{G,OFF} = 2.5 \, \Omega$) as depicted in Figure 10 and 11 were carried out in a double-pulse test using a half-bridge topology setup at room temperature with an initial DC-link voltage of 800 V. The adjusted load current is either nominal current (300 A) or twice nominal current (600 A).

Figure 10: Turn-On Behavior at $V_{DC} = 800 \, V$
Figure 11: Turn-Off Behavior at $V_{DC} = 800$ V
Short Circuit Behavior

The measurement examples shown with the SiC power module Wolfspeed CAS300M12BM2 ($R_{\text{G,ON}} = 2.5 \Omega$ and $R_{\text{G,OFF}} = 2.5 \Omega$) as depicted in Figure 12 were carried at room temperature with an initial DC-link voltage of 800 V.

![Graphs showing short circuit behavior for different channels](https://gate-driver.power.com/)

**Figure 12:** Short Circuit Behavior at $V_{\text{DC}} = 800$ V
Handling

To avoid possible failures caused by ESD, a handling- and assembly-process with persistent ESD protection is necessary /1/.

References

/1/ Application Note AN-0902, Avoiding ESD with CONCEPT Drivers, Power Integrations

History

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
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<td>2019-04-04</td>
<td>A.1</td>
<td>Initial Version</td>
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<tr>
<td>2019-09-10</td>
<td>A.2</td>
<td>Pinning corrected in Figure 1, History added</td>
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</table>
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<th>Germany (Gate Driver Sales)</th>
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<th>Italy</th>
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<th>Singapore</th>
<th>Taiwan</th>
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